

MS-7680

Ver: 5.2

m-ATX : 243.8 * 195 mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UP1625 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: IP6103

CPU SA : OP+MOS

DDR: UP6103

PCH: UP6103

ACPI:

UPI

Other:

SATA2.0 x4 (PCH)

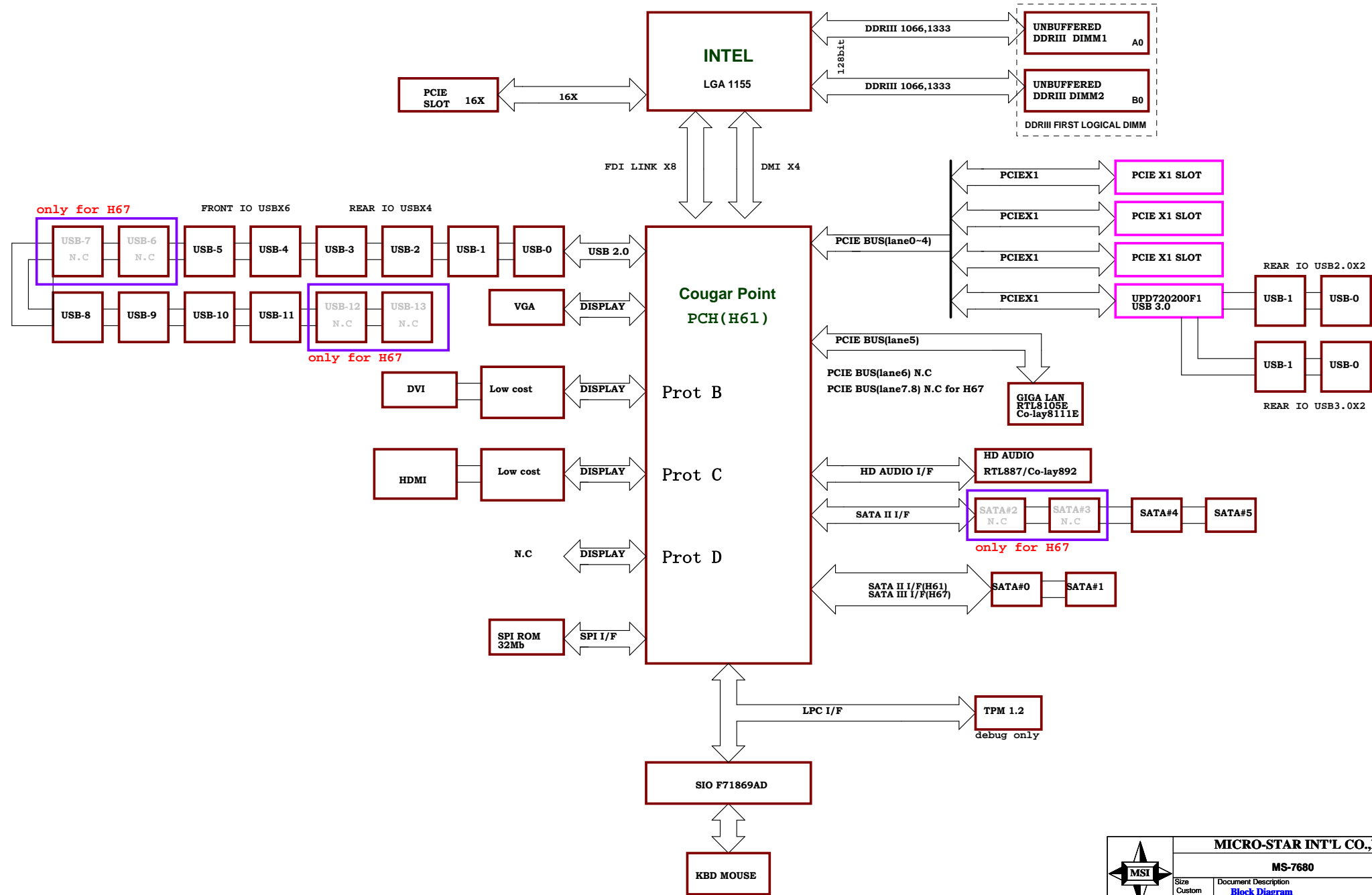
USB2.0 RearX4 Front x6

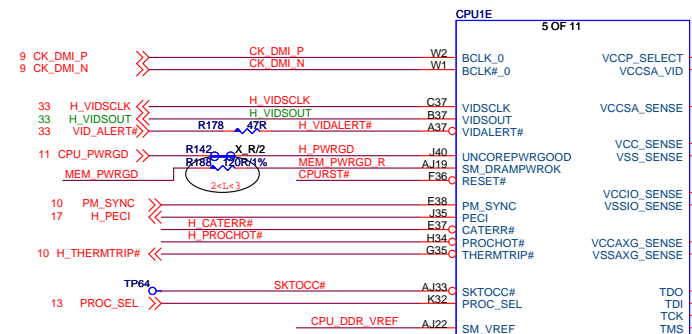
D-SUB/DVI*1

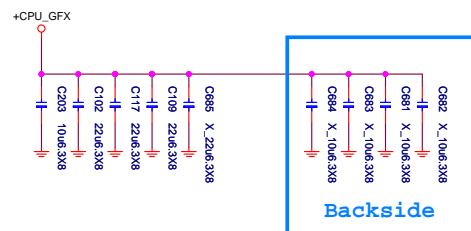
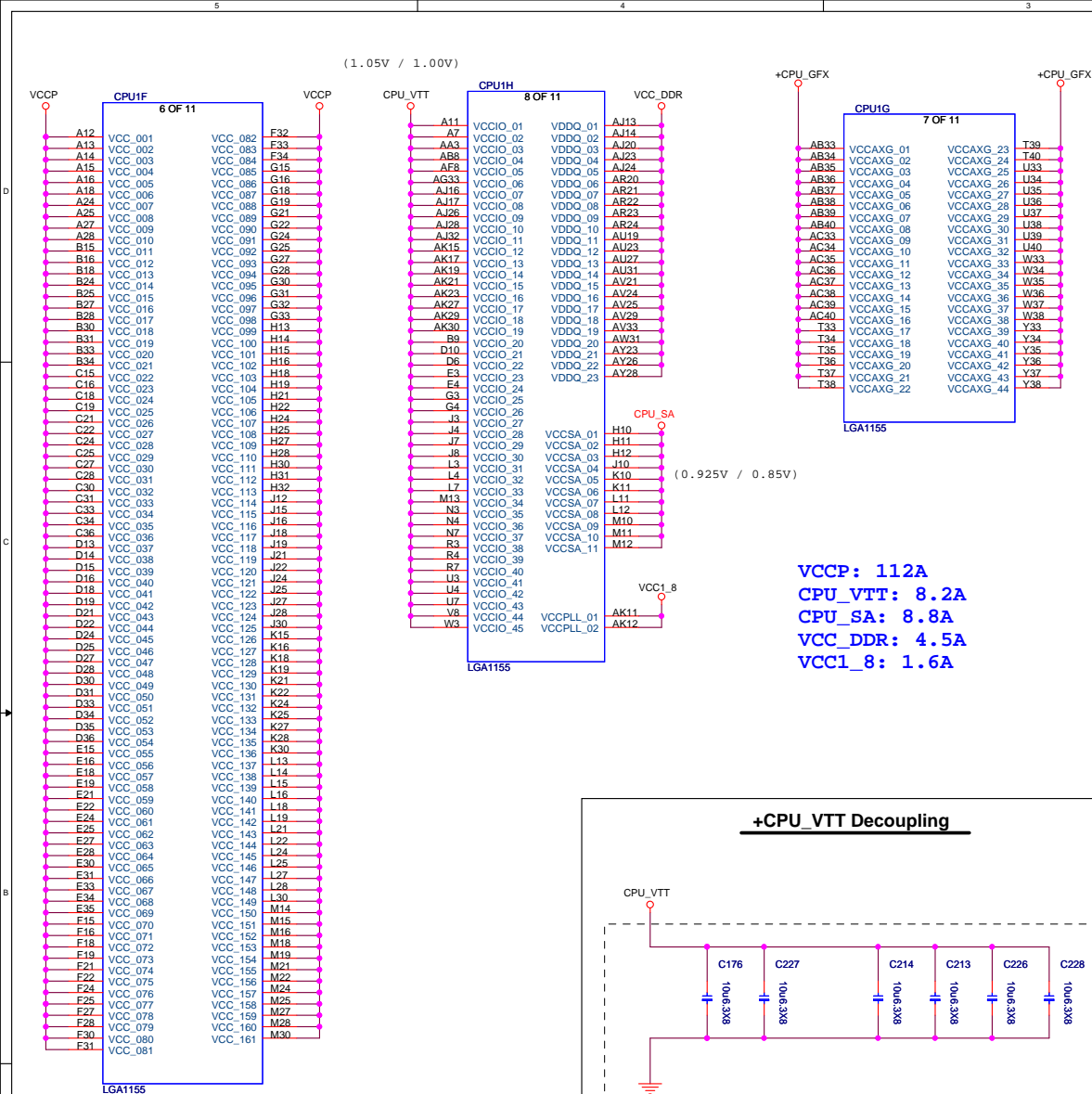
TPM Header *1

on BOARD BUZZER

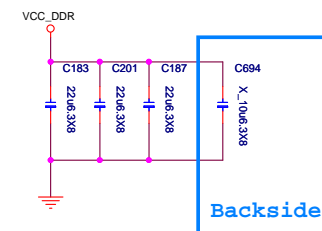
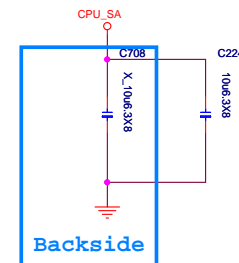
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CPU-GND	6
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CP-SATA/HOST/FAN/GPIO/VGA	10
CP-SMB/LPC/AUDIO/RTC	11
CP-POWER	12
CP-GND/NVRAM	13
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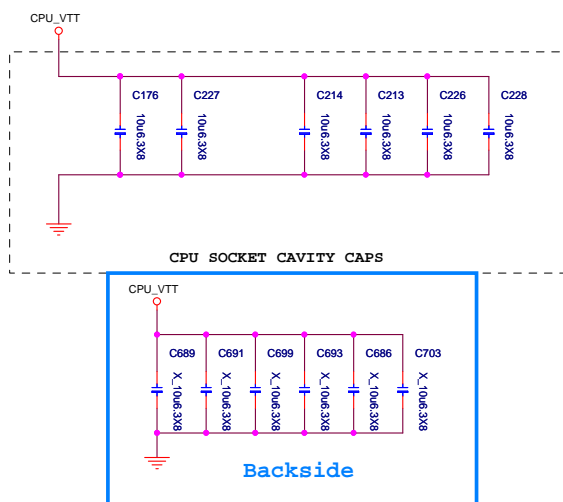


CPU SOCKET CAVITY
CAPS

+1.5V_DDR3-Decoupling

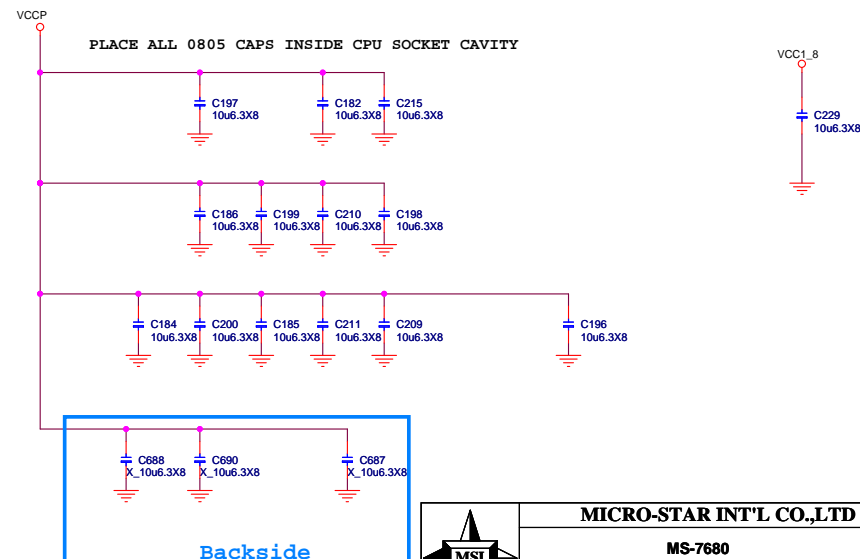
CPU SOCKET CAVITY
CAPS

+CPU_VTT Decoupling



+CPU_VCCP-Decoupling

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY

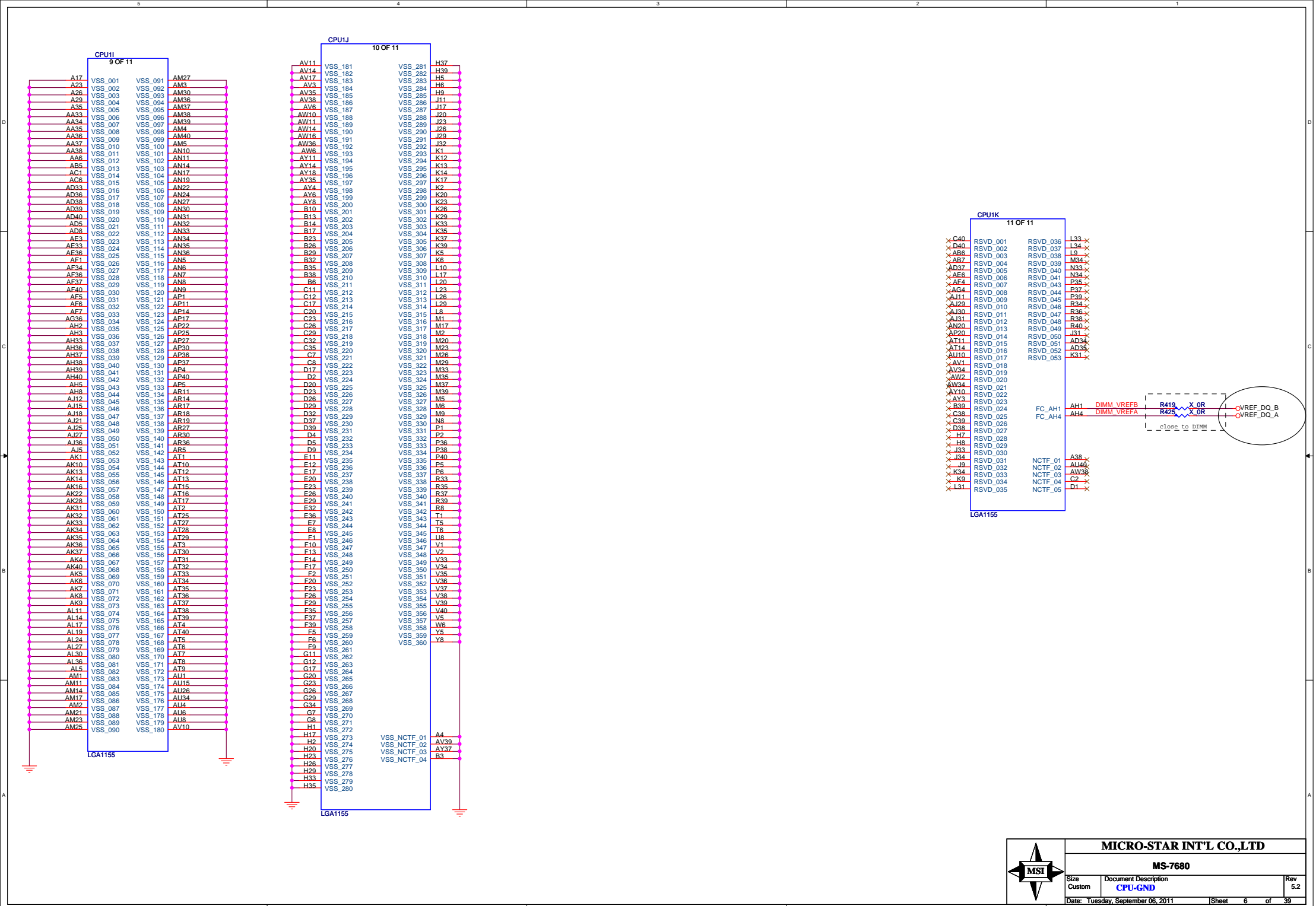


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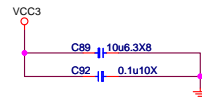
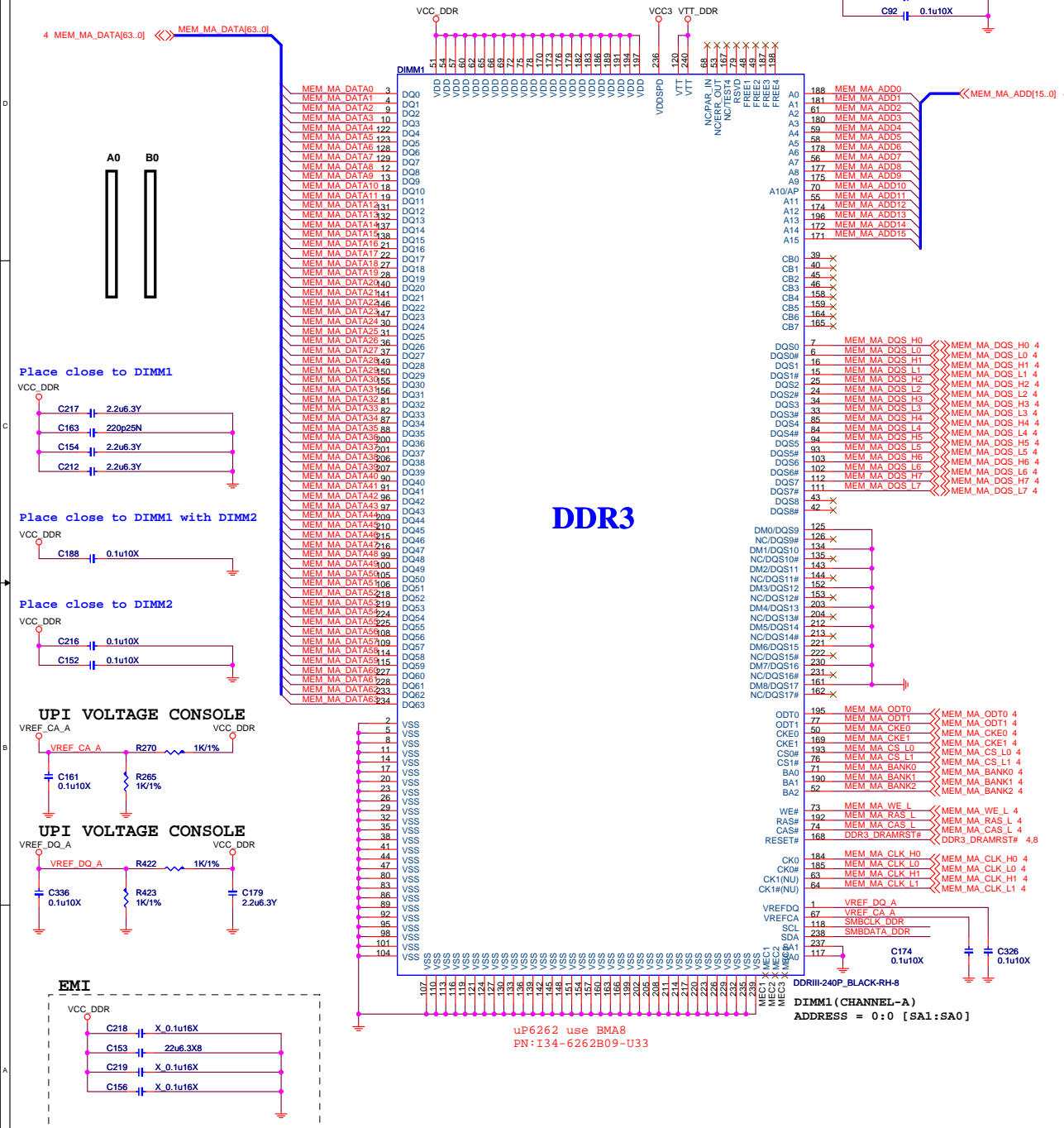
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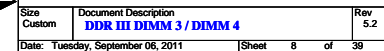
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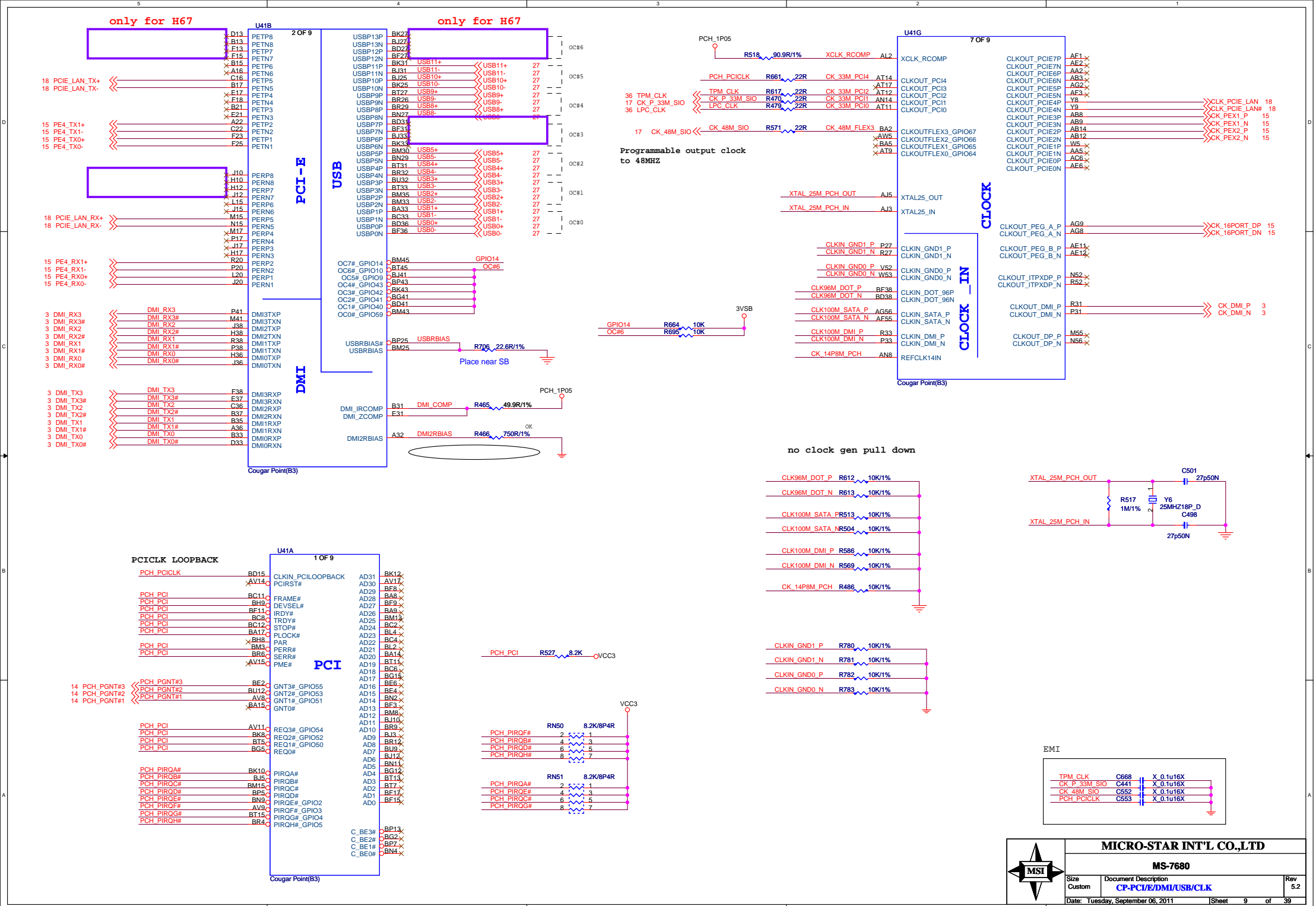


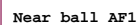
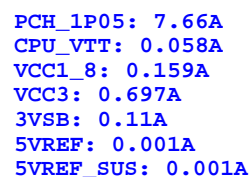
DDRIII DIMM_A0

DDRIII DIMM_A1



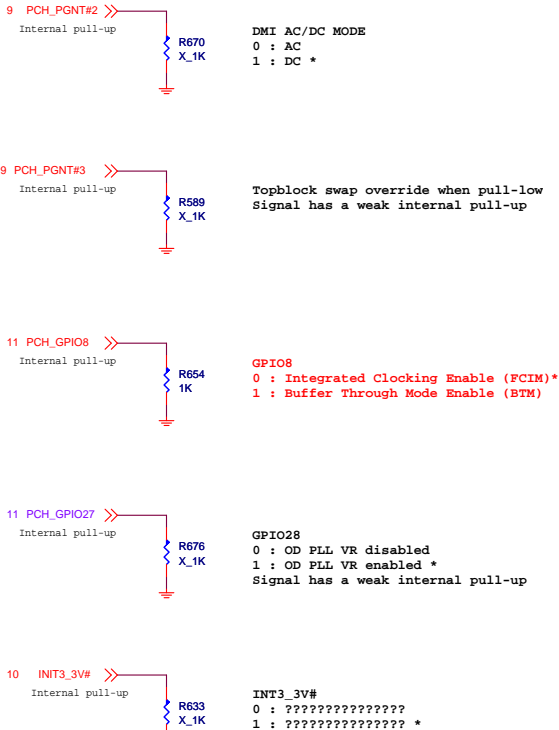
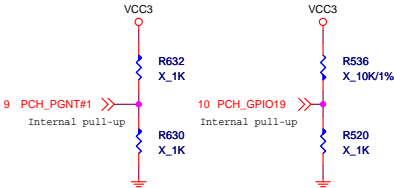




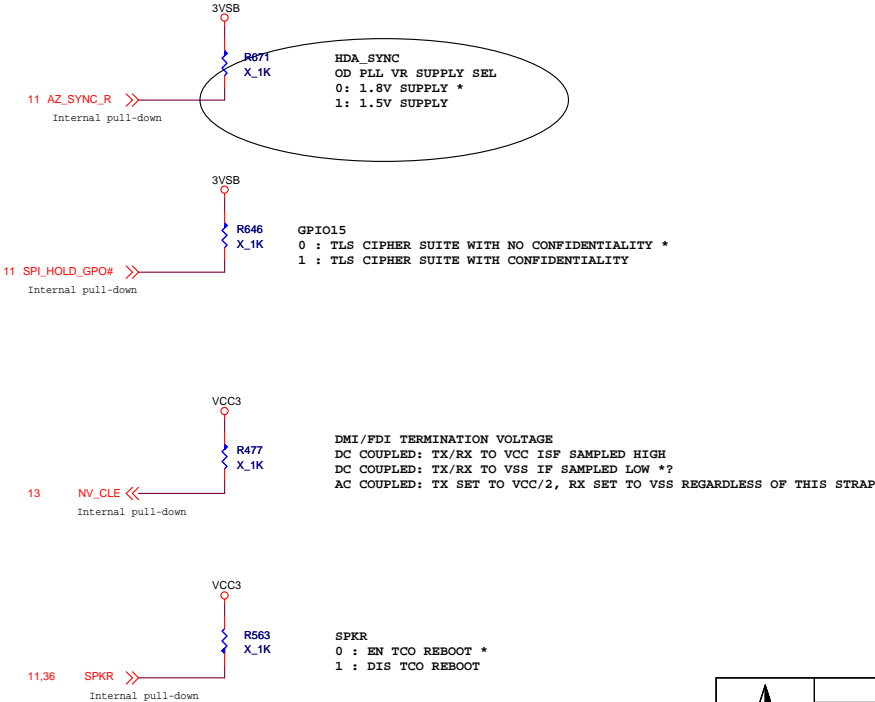
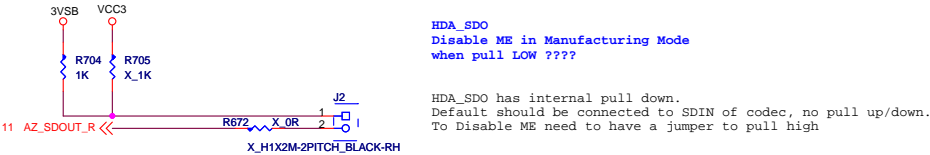
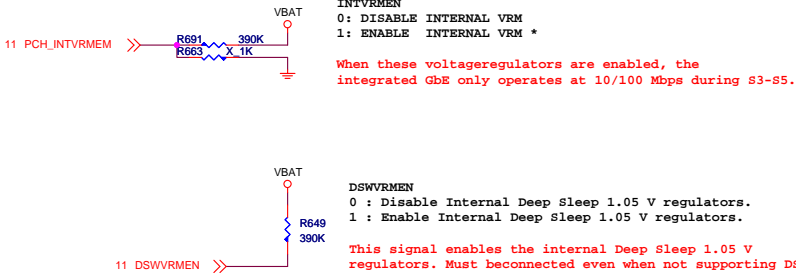


PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

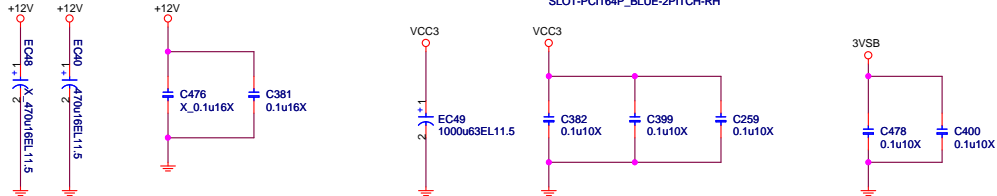
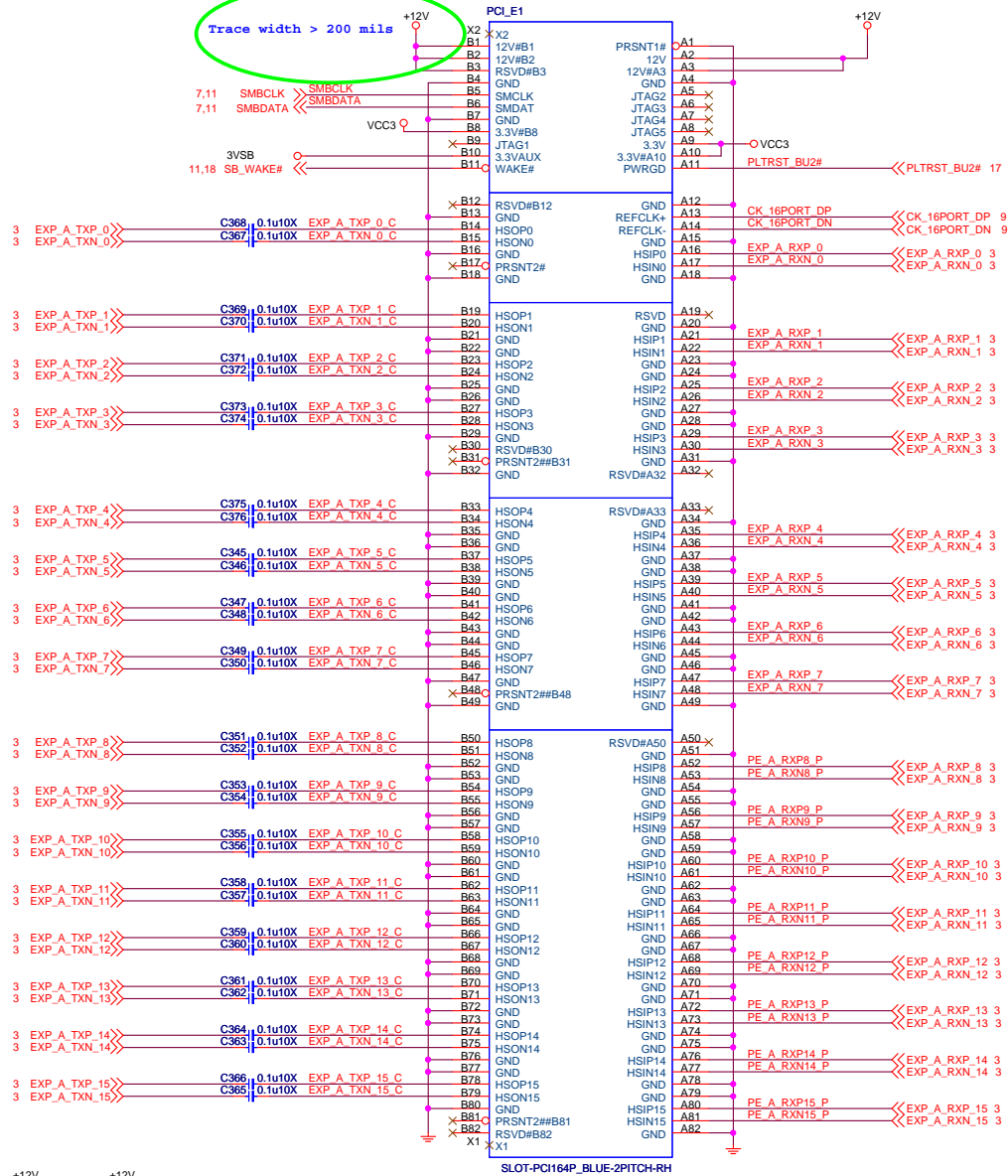


1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

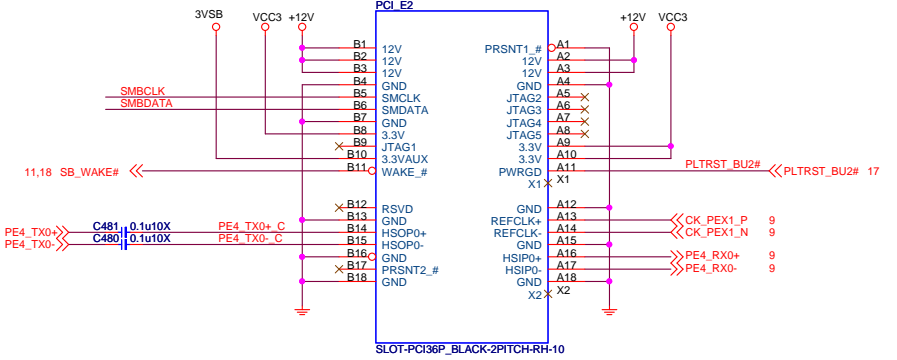


PCI_Express X16 Slot

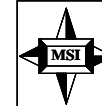
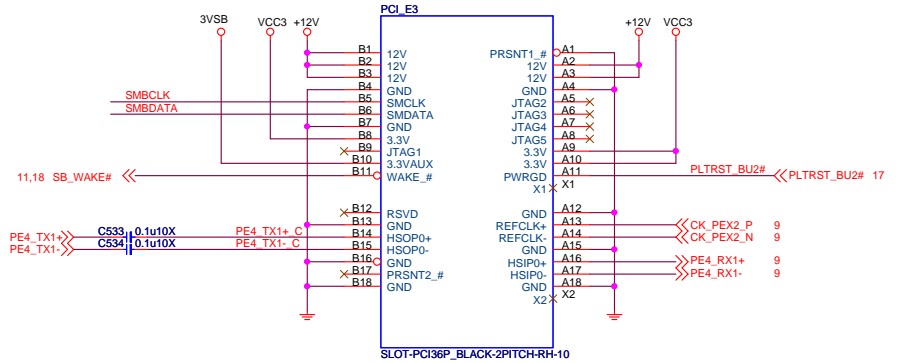
N11-1640971-K06



PCI EXPRESS x1-PORT



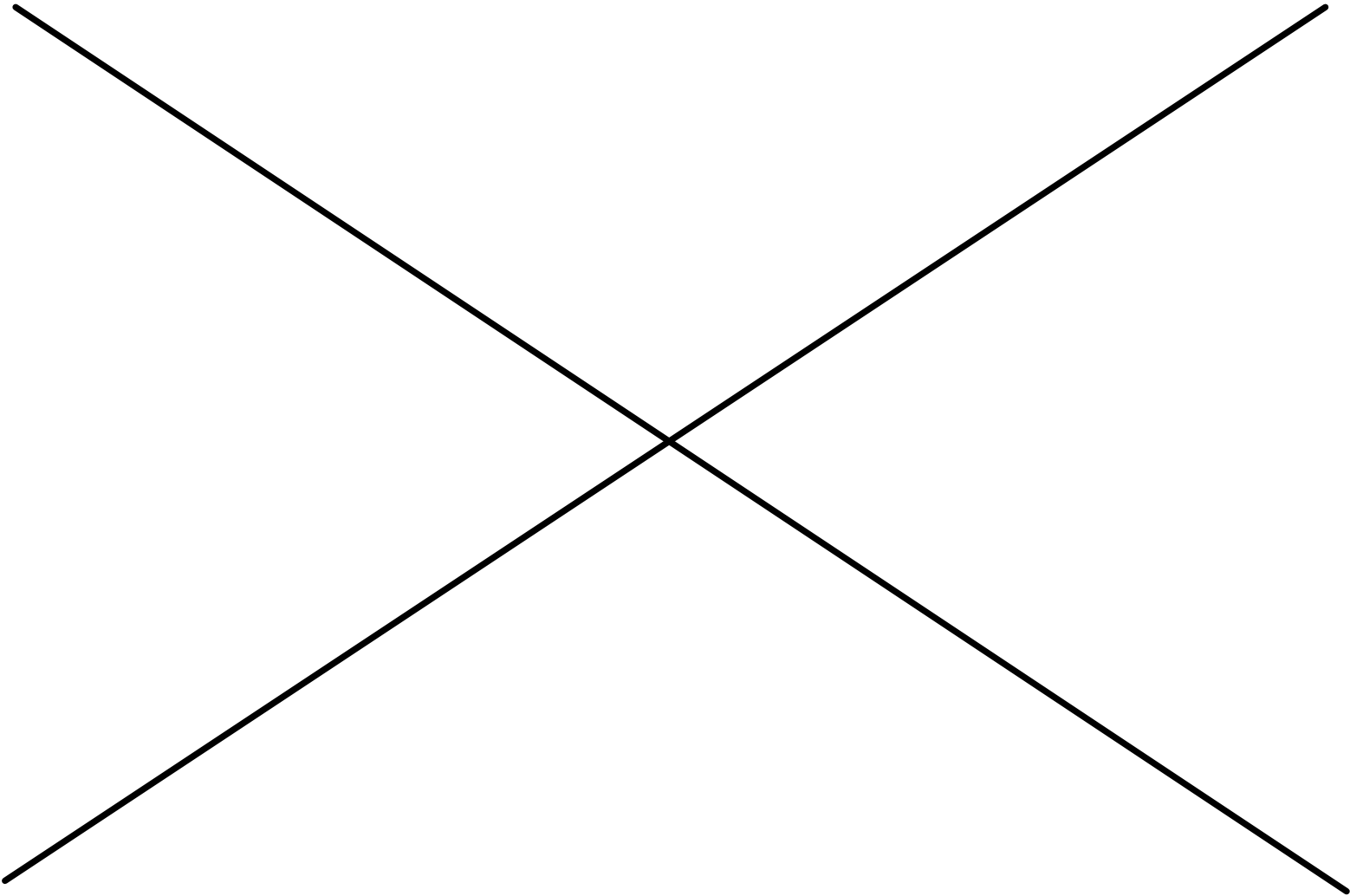
PCI EXPRESS x1-PORT

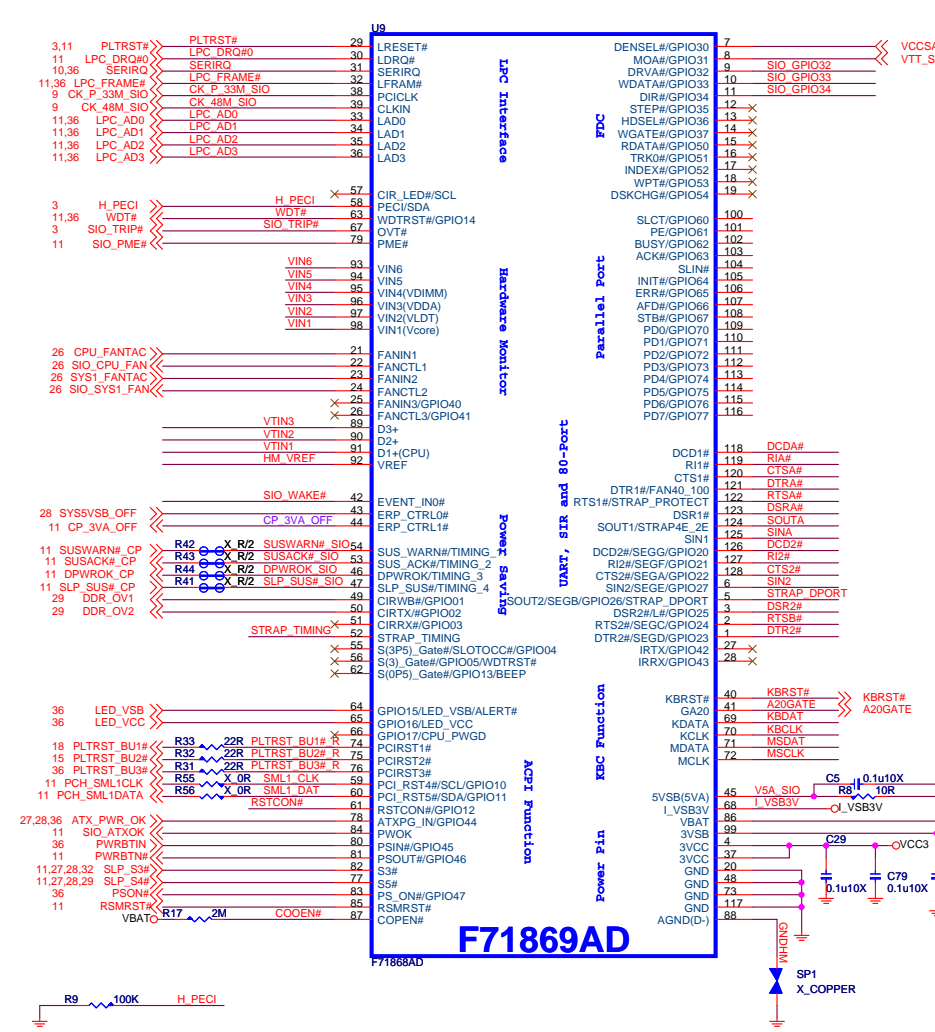


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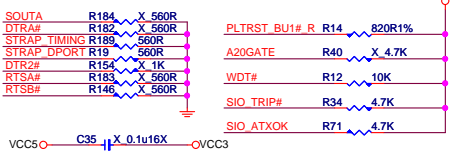
Size Custom	Document Description PCIE x16 /x1/x1	Rev 5.2
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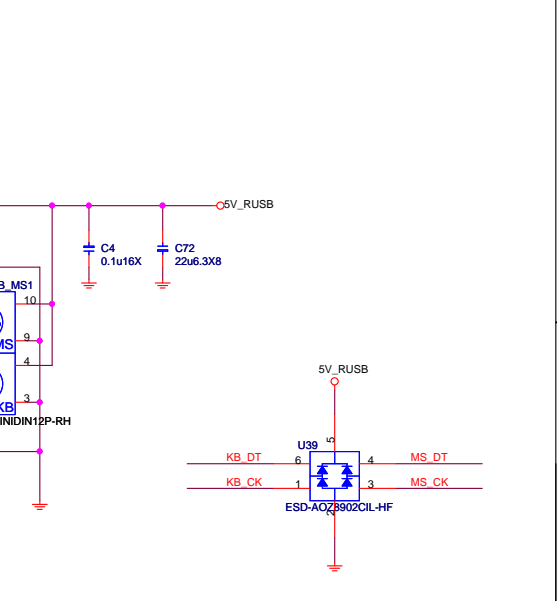
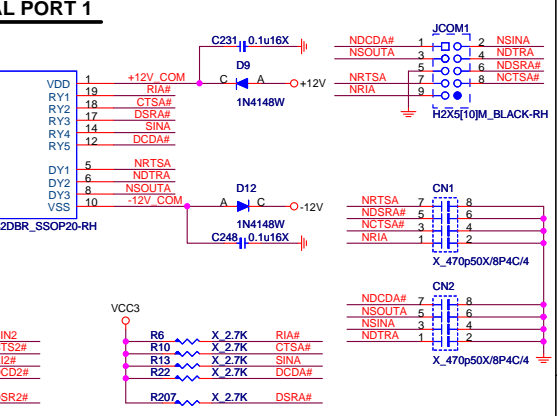
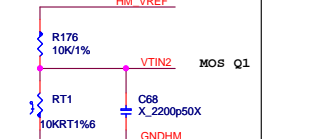
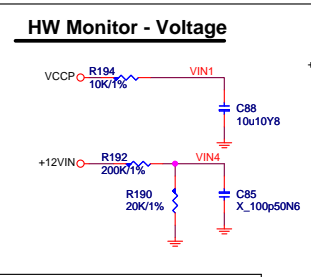
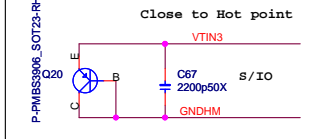
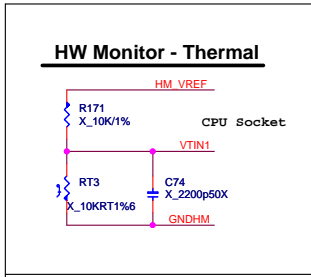
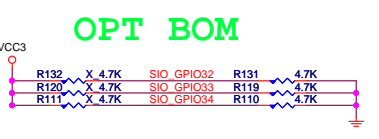


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA#	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		

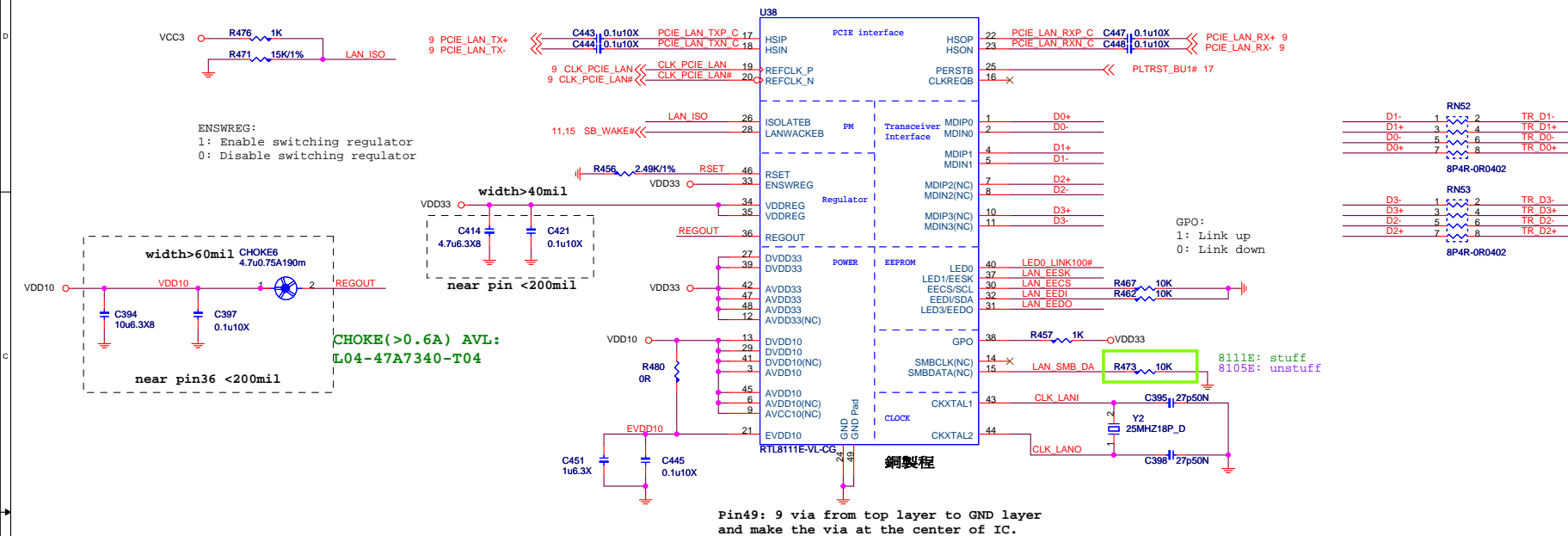


GPIO34 / GPIO33 / GPIO32	0	0	0	SKU_A
	0	0	1	SKU_B
	0	1	0	SKU_C
	0	0	1	SKU_D

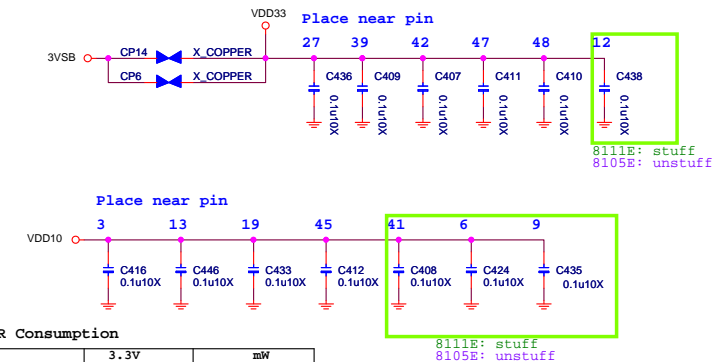


RTL8111E Giga LAN

RTL8105E 10/100M LAN



3.3v Power on rise time : 1-100ms. MAX: 163mA



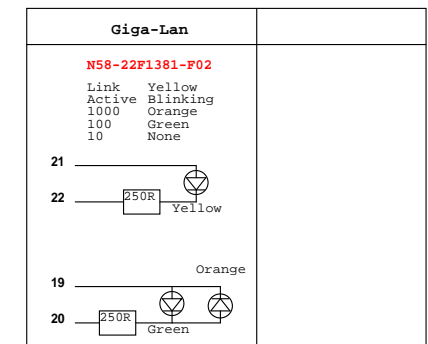
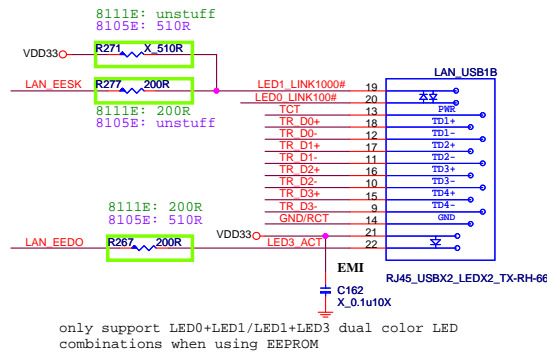
8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
SO ALDPS	3.2	11

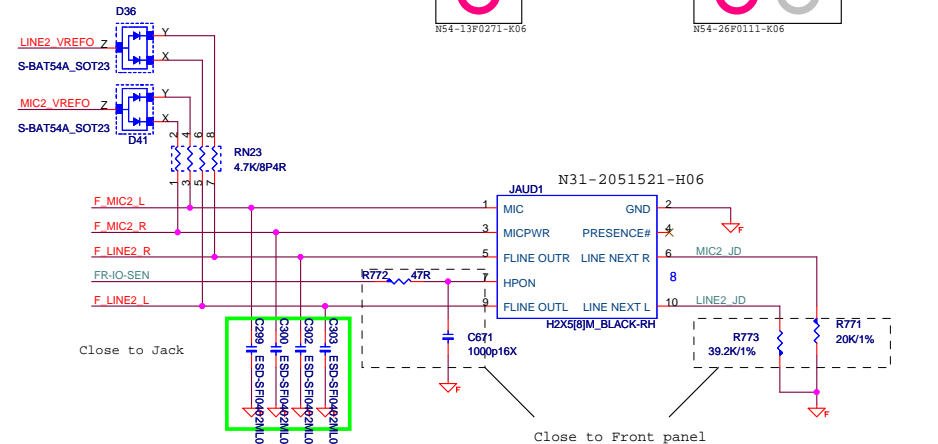
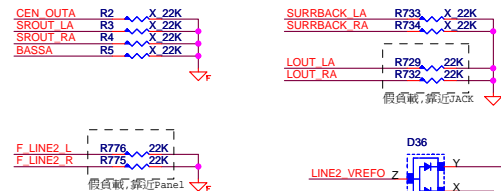
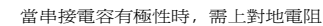
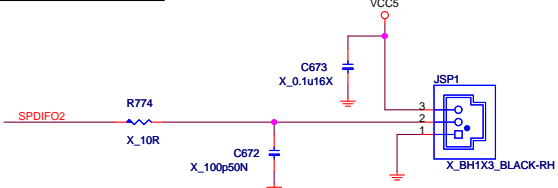
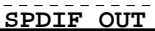
8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

LAN Connector



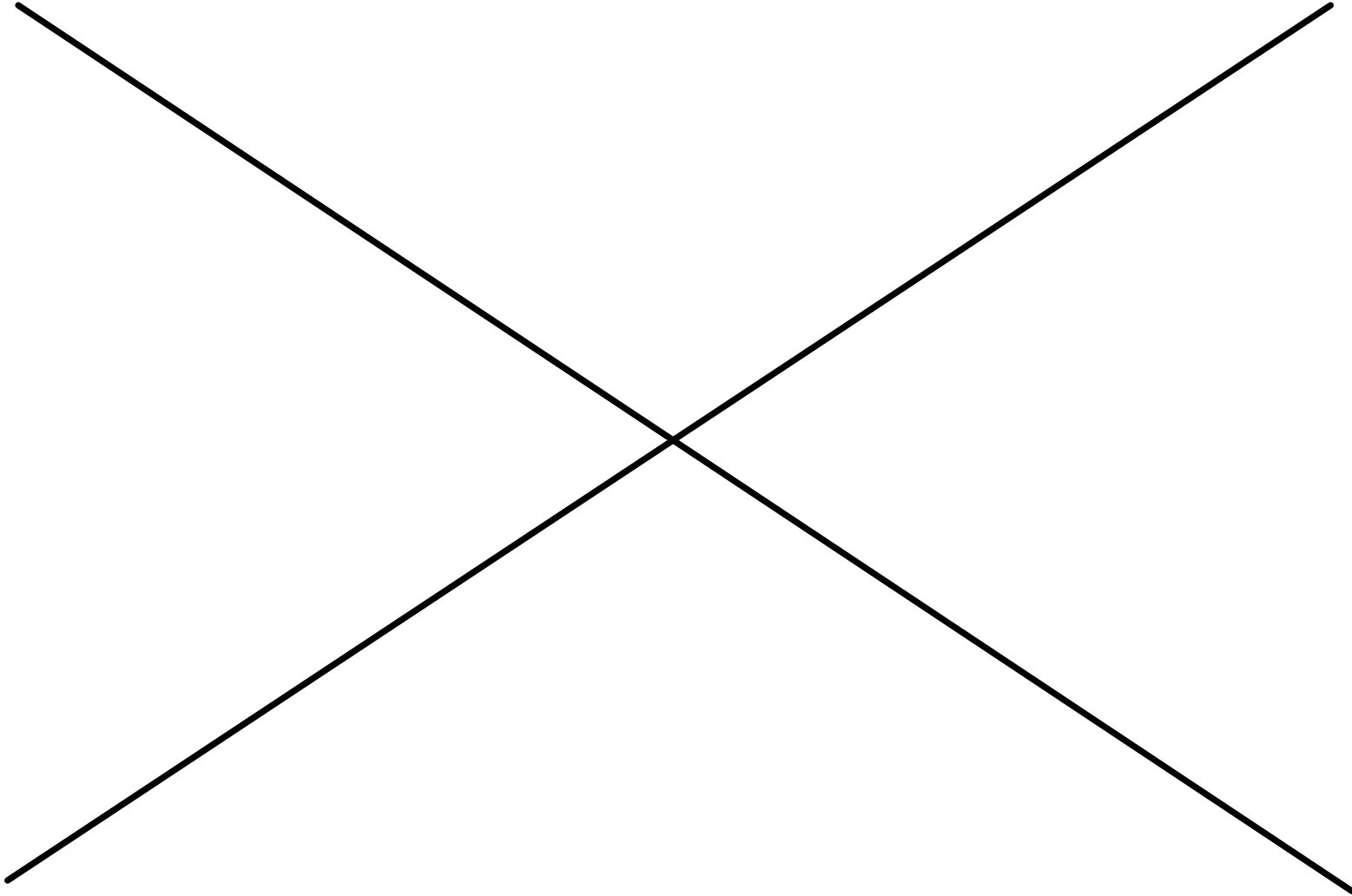
ALC892

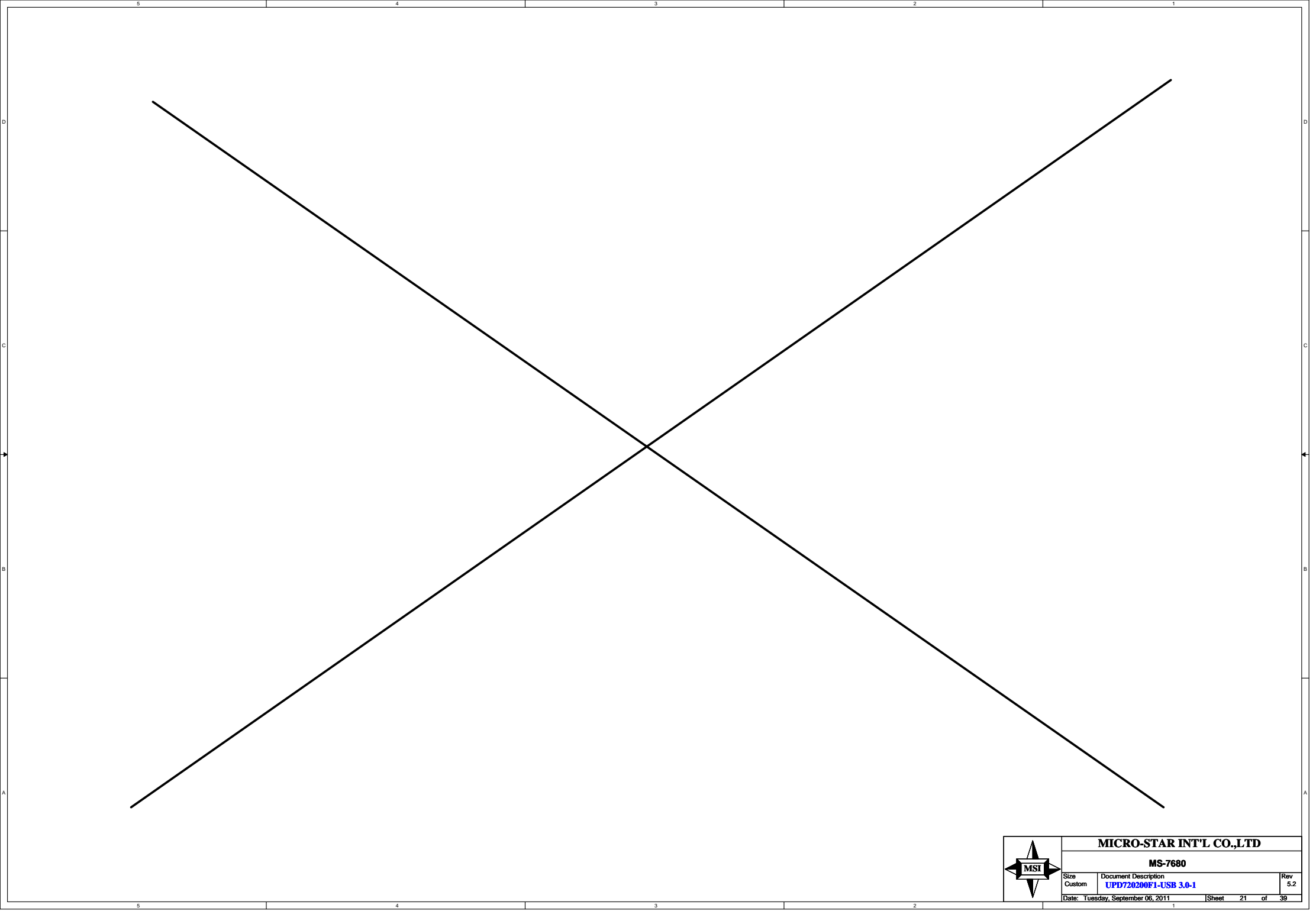


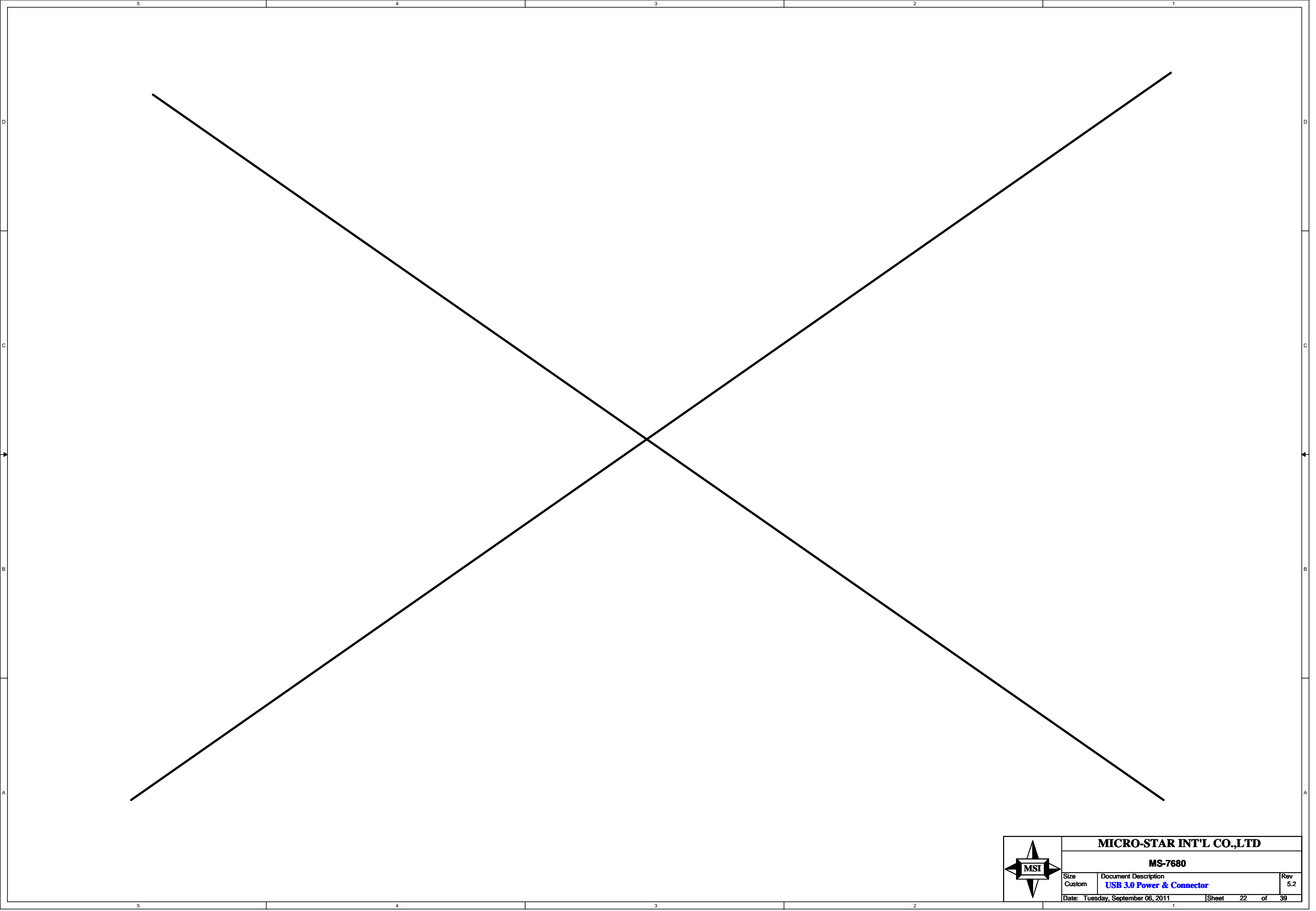
Varister --> cap for cost down

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Size Custom	Document Description ALC892_COLAY_ALC887VD	Rev 5.2
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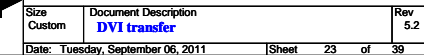
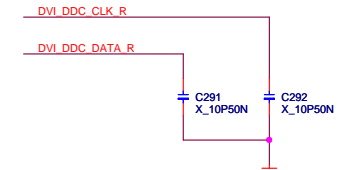


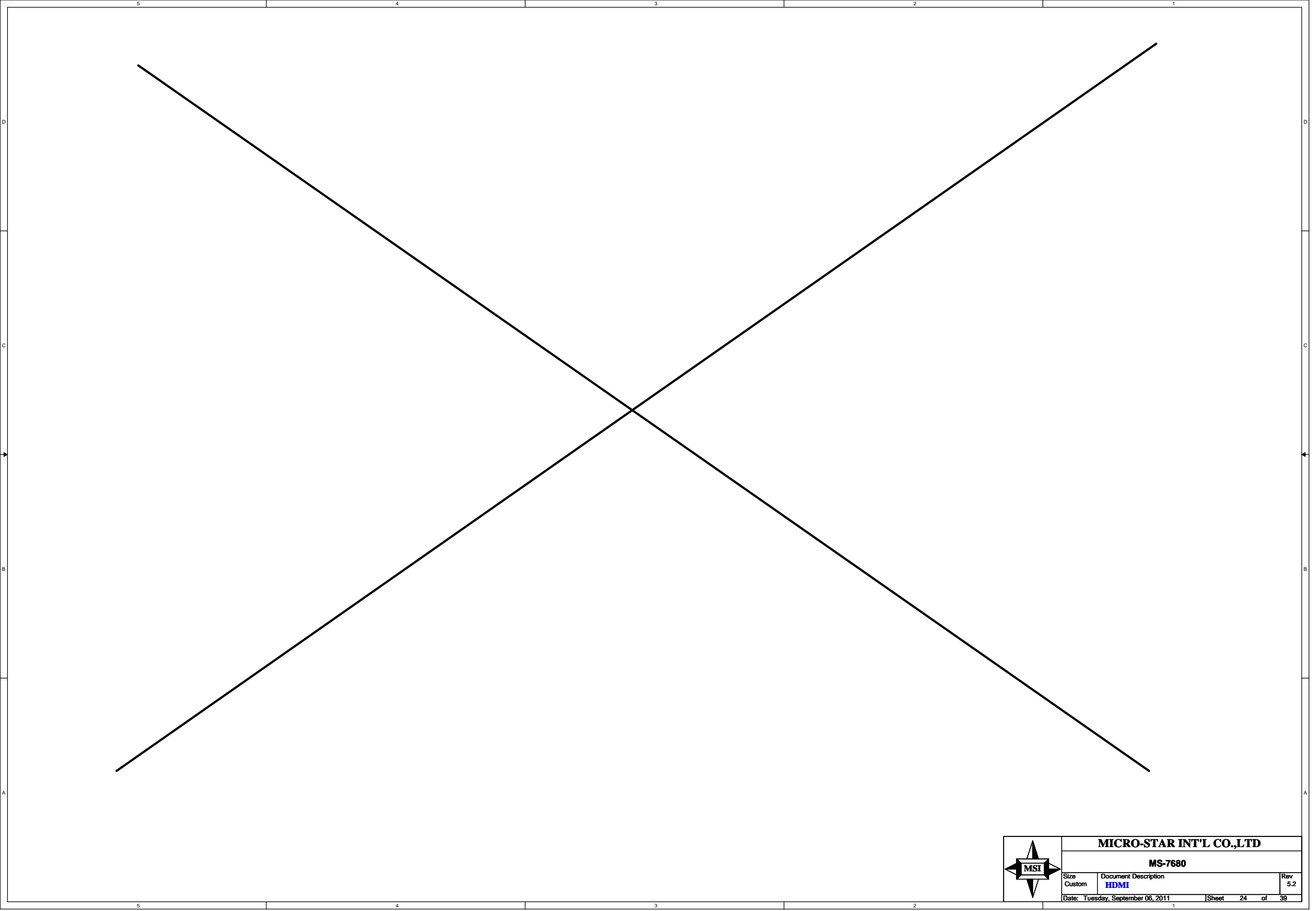
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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)





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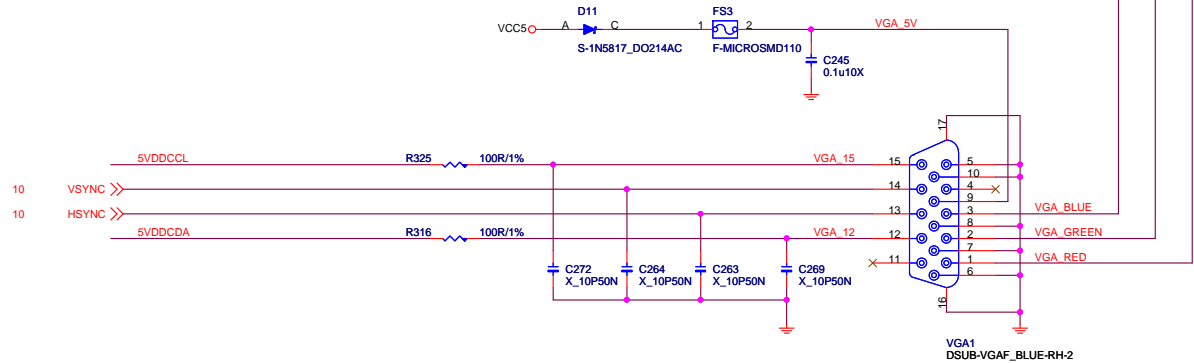
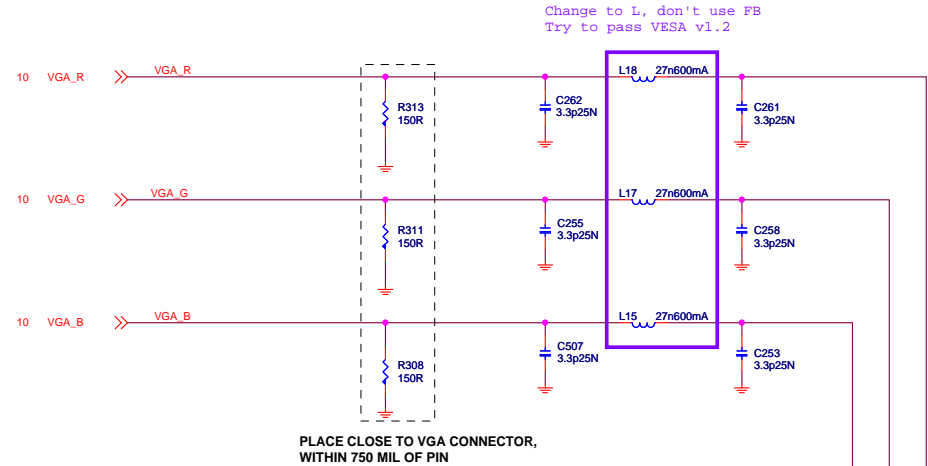
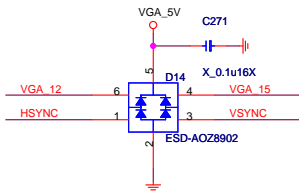
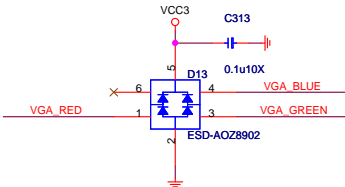
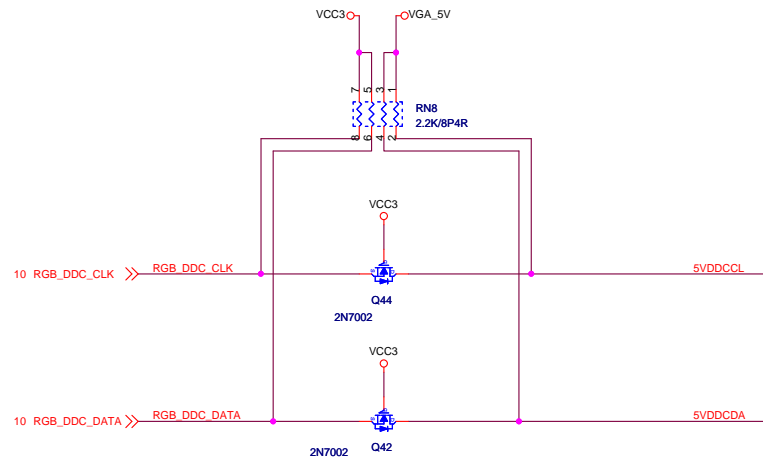
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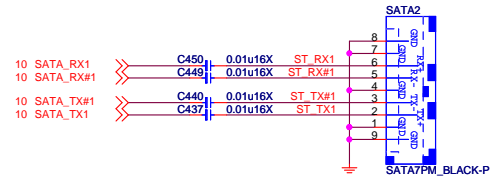
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

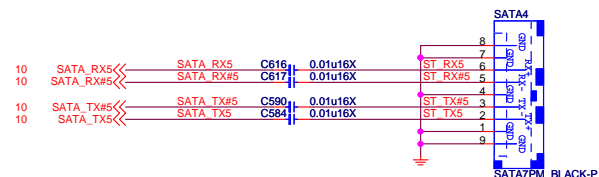
Level shift



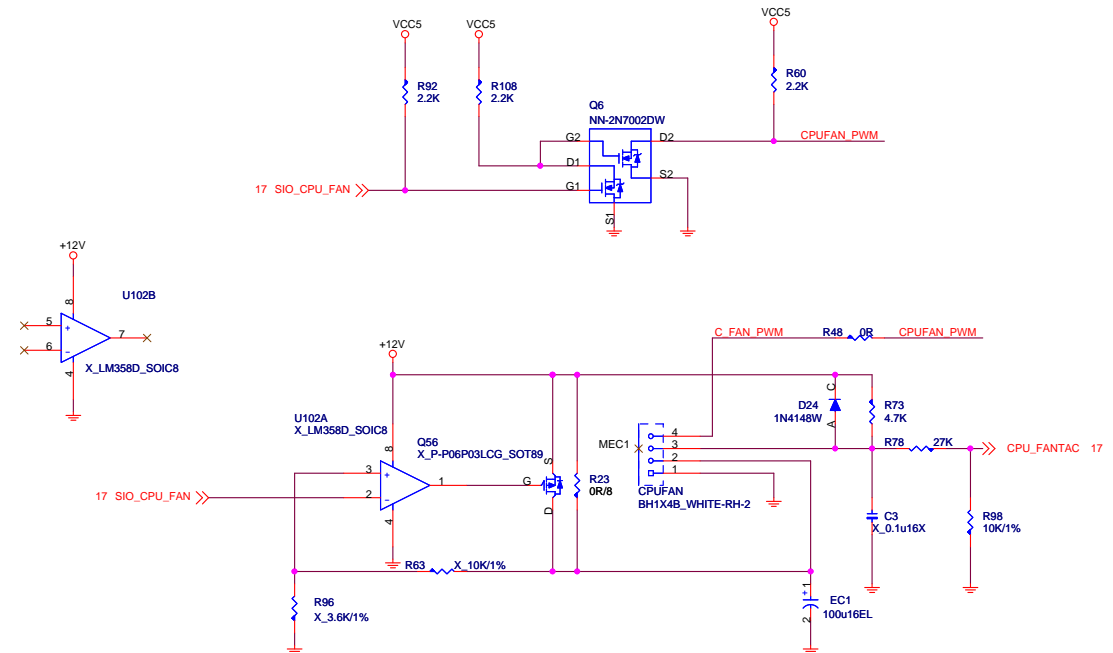
H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G



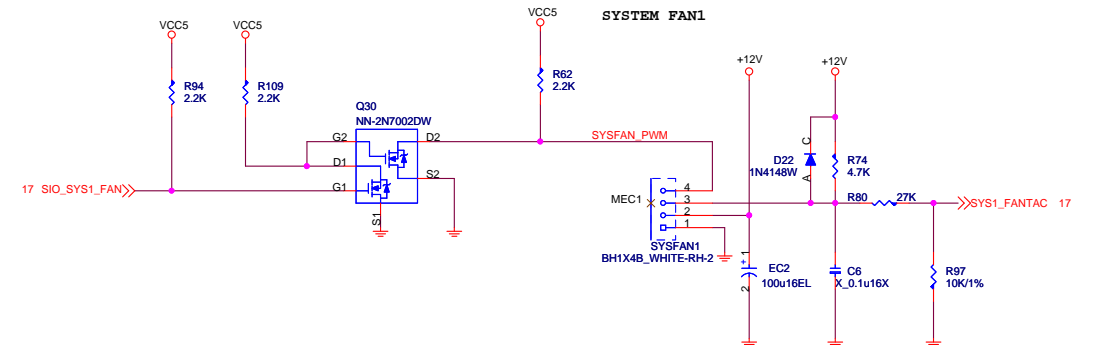
For H61,SATA2&3 removed



PWM/DC MODE Co-lay

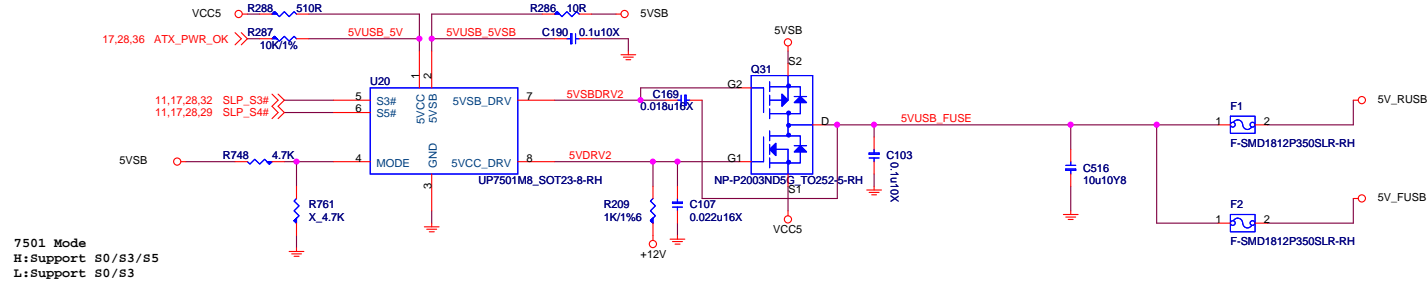


SYSTEM FAN1

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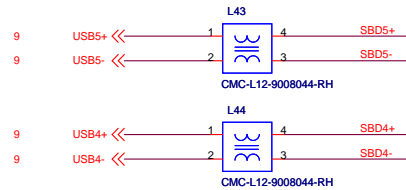
5V_RUSB Switch



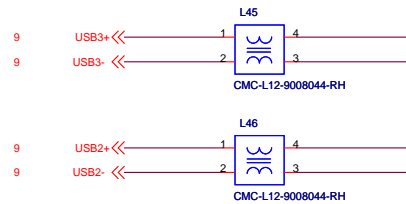
Front USB Connector

For H61 6,7,12,13 Port should be remove

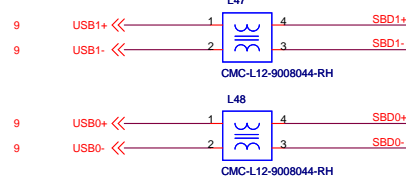
FRONT USB PORT 4,5



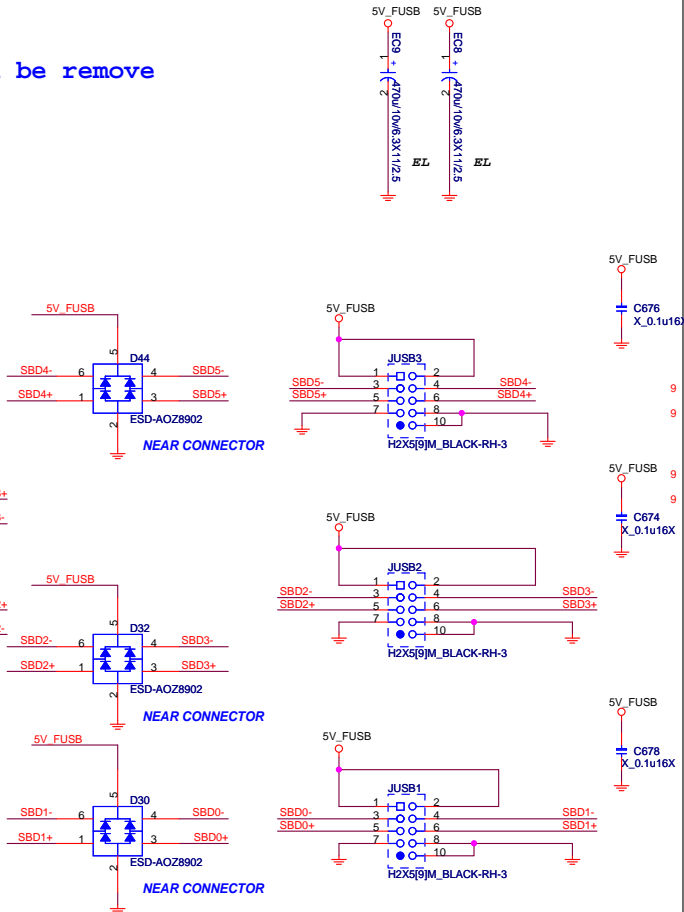
FRONT USB PORT 2,3



FRONT USB PORT 0,1

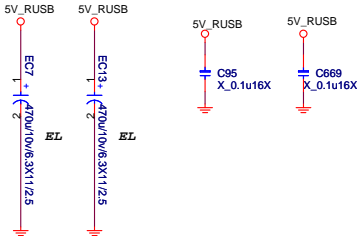


NEAR USB Front CONNECTOR

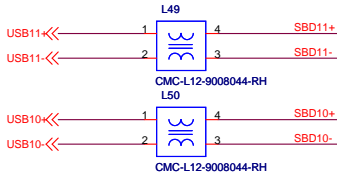


Rear USB Connector

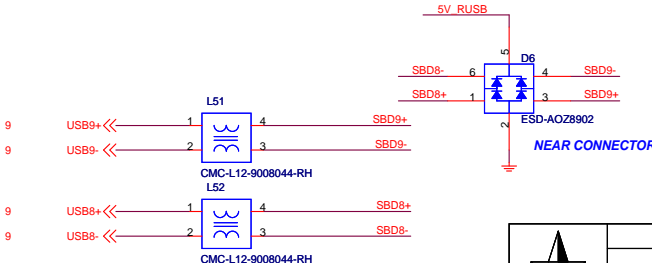
NEAR USB REAR CONNECTOR



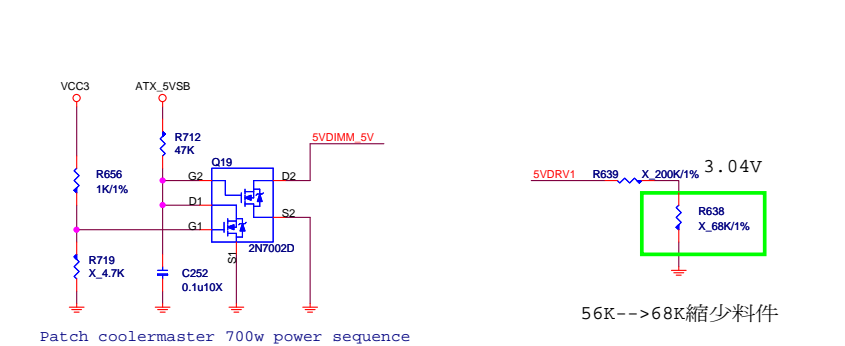
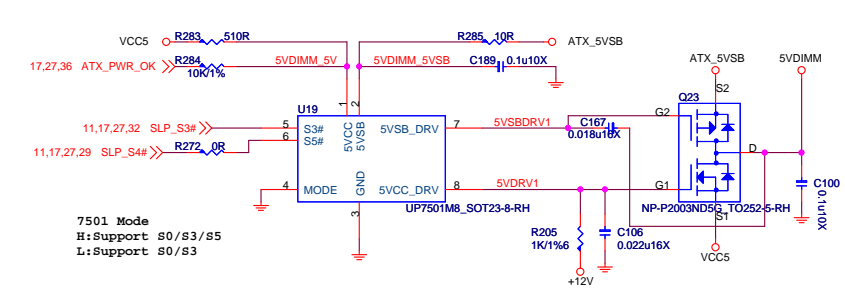
REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9 (With PS2)



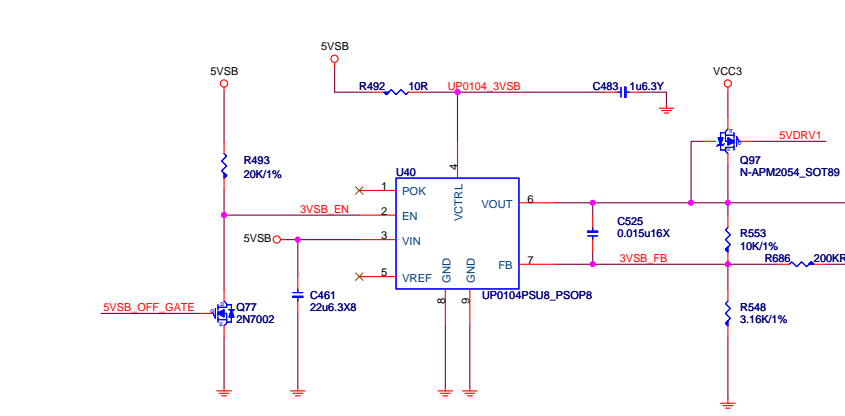
5VDIMM FOR DDR



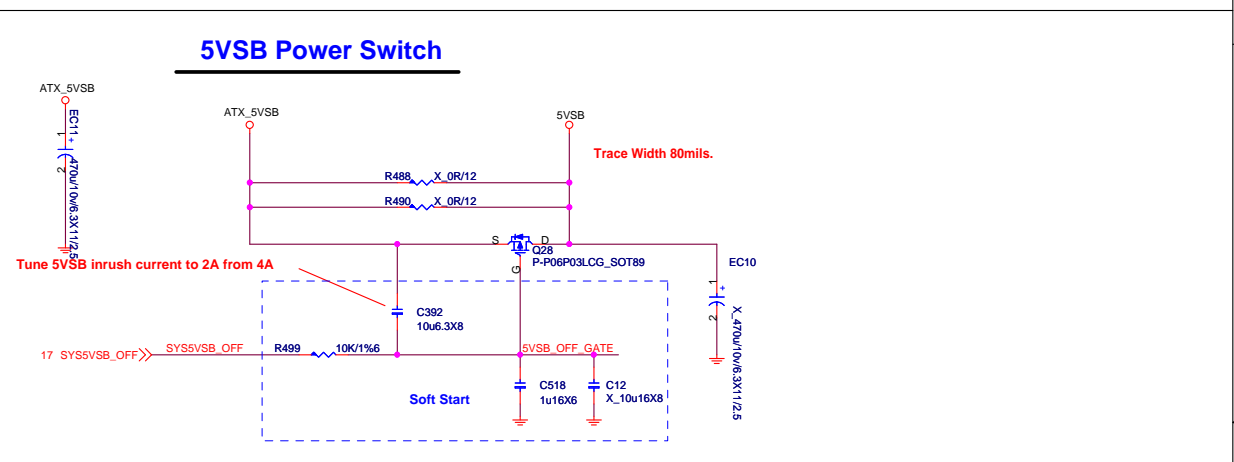
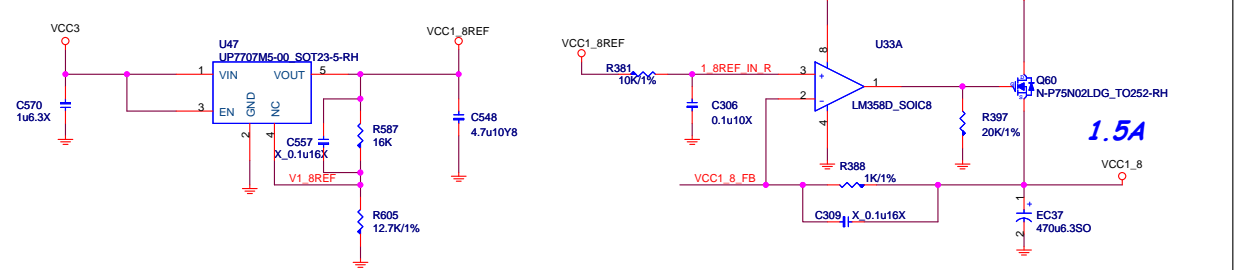
Patch coolermaster 700w power sequence

3VSB

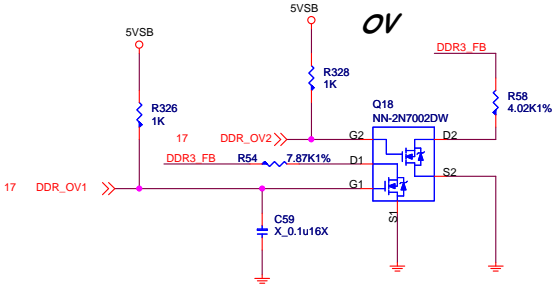
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



VCC1_8REF



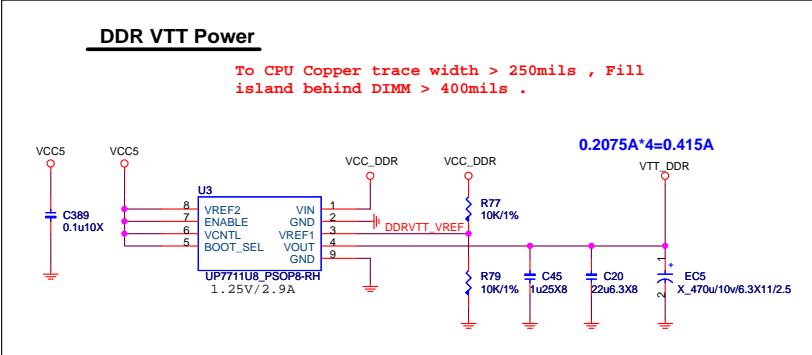
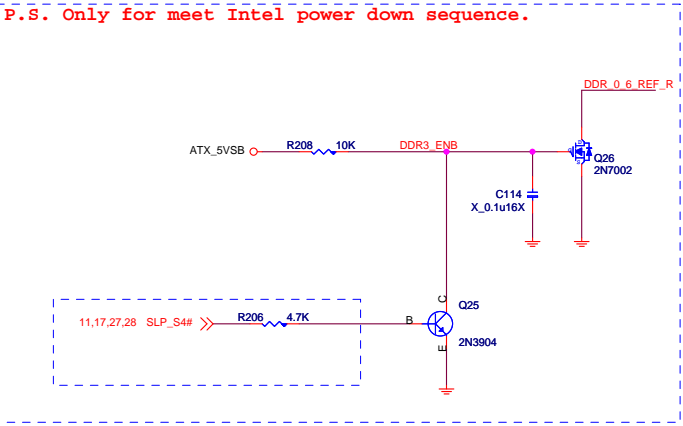
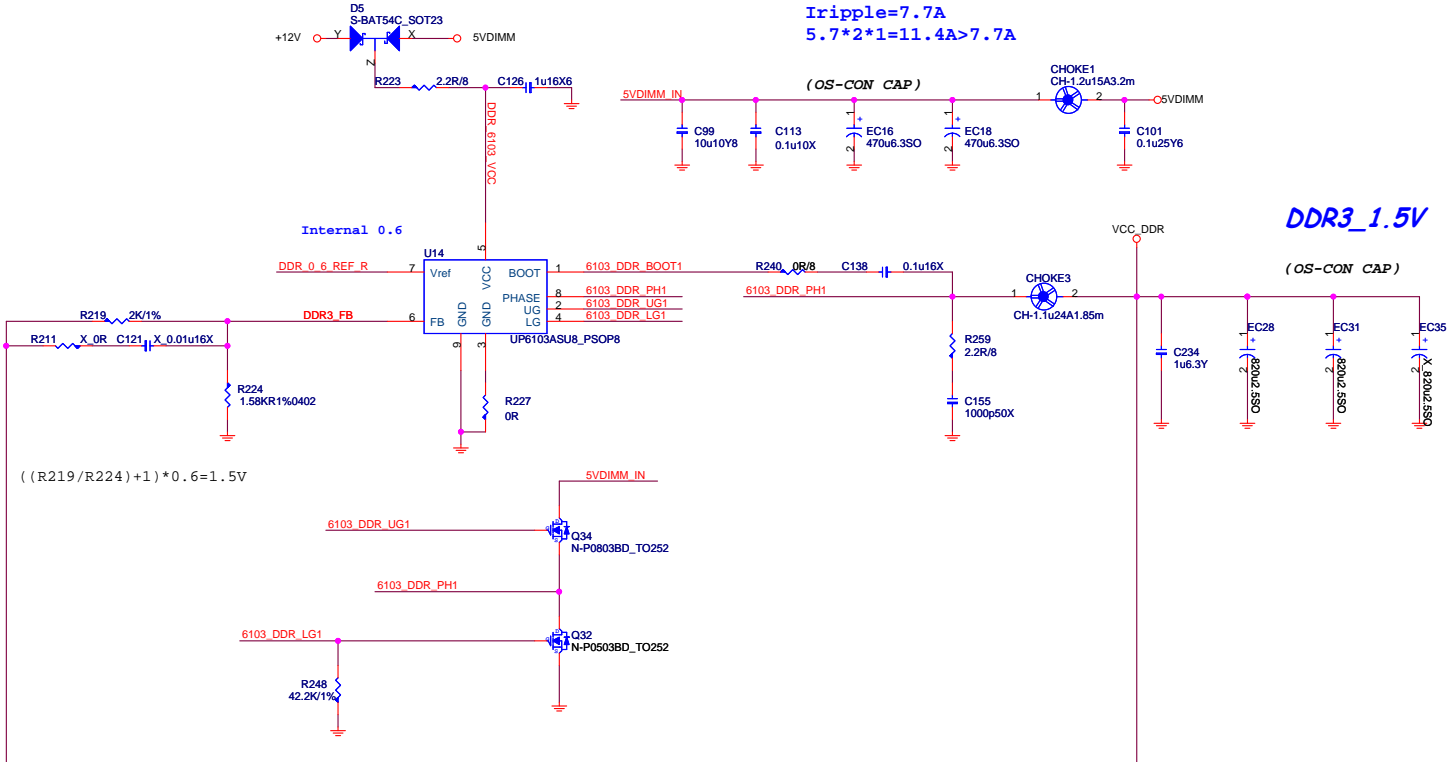
DDR3_1.5V 4.5A+7.5A+1A=13A
4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT



*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
 DDR_OV2 = GPIO02(S/IO)

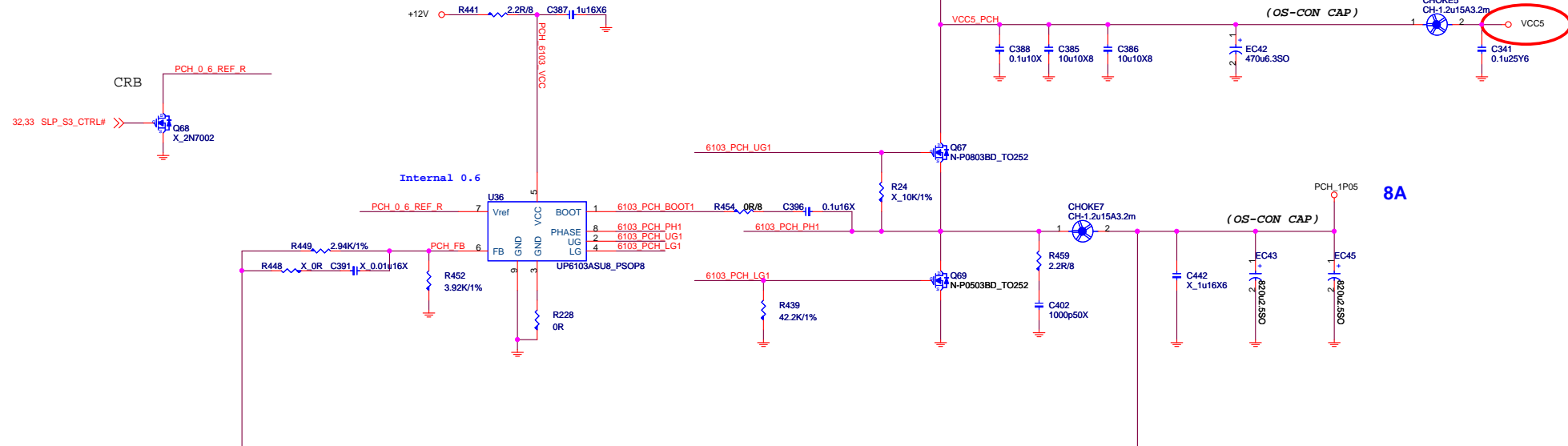


PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

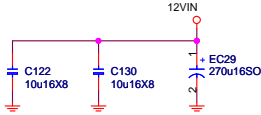
1.8A FOR ME CORE



CPU_VTT:1.05/1.00

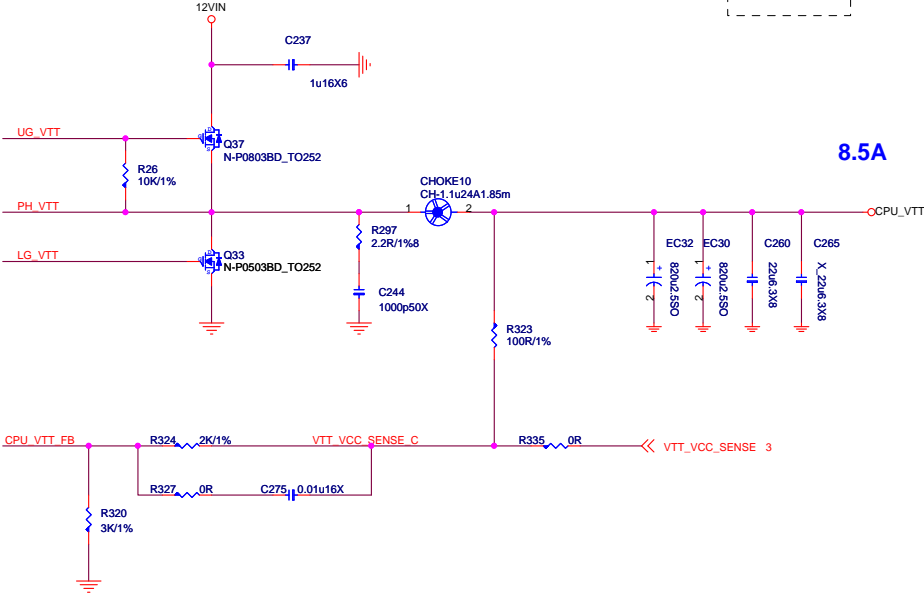
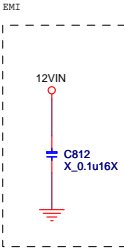
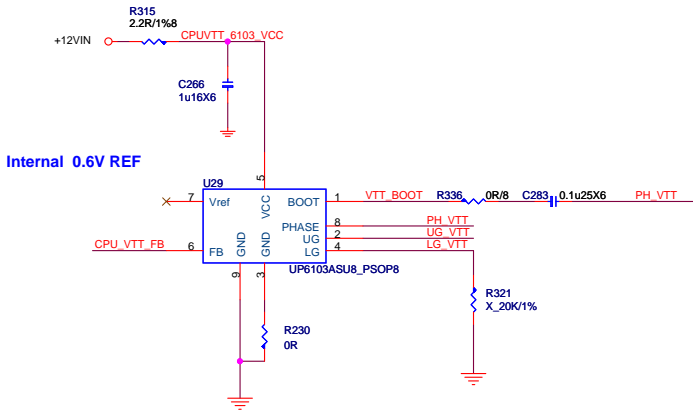
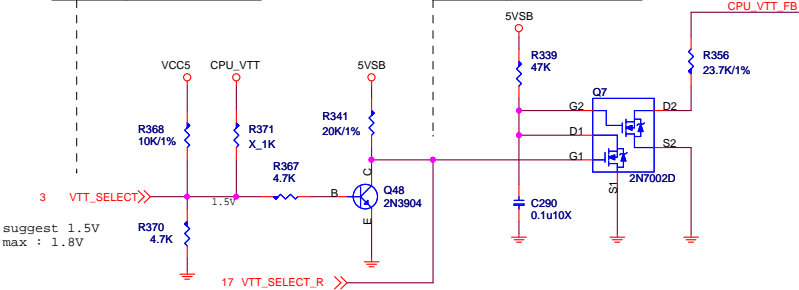
CPU VTT 8.5A + SA Core =8.8A =17.3A

$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$
 $5 \times 1 = 5A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.0V

VTT_SELECT Table	
Low	1.05V
High	1.0V



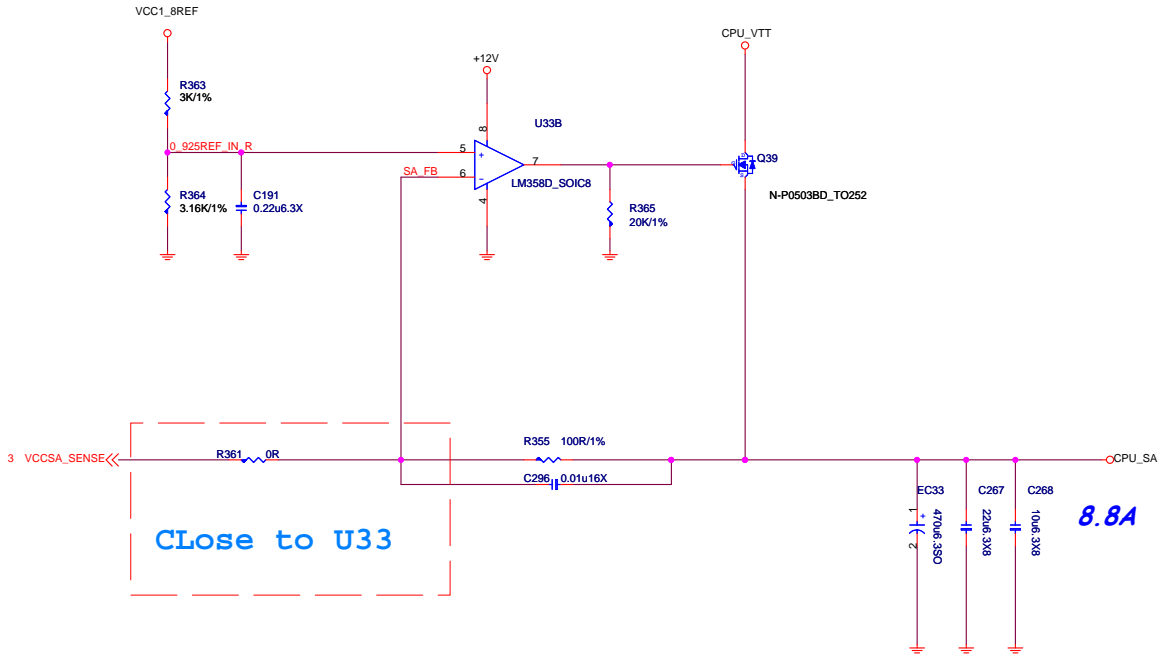
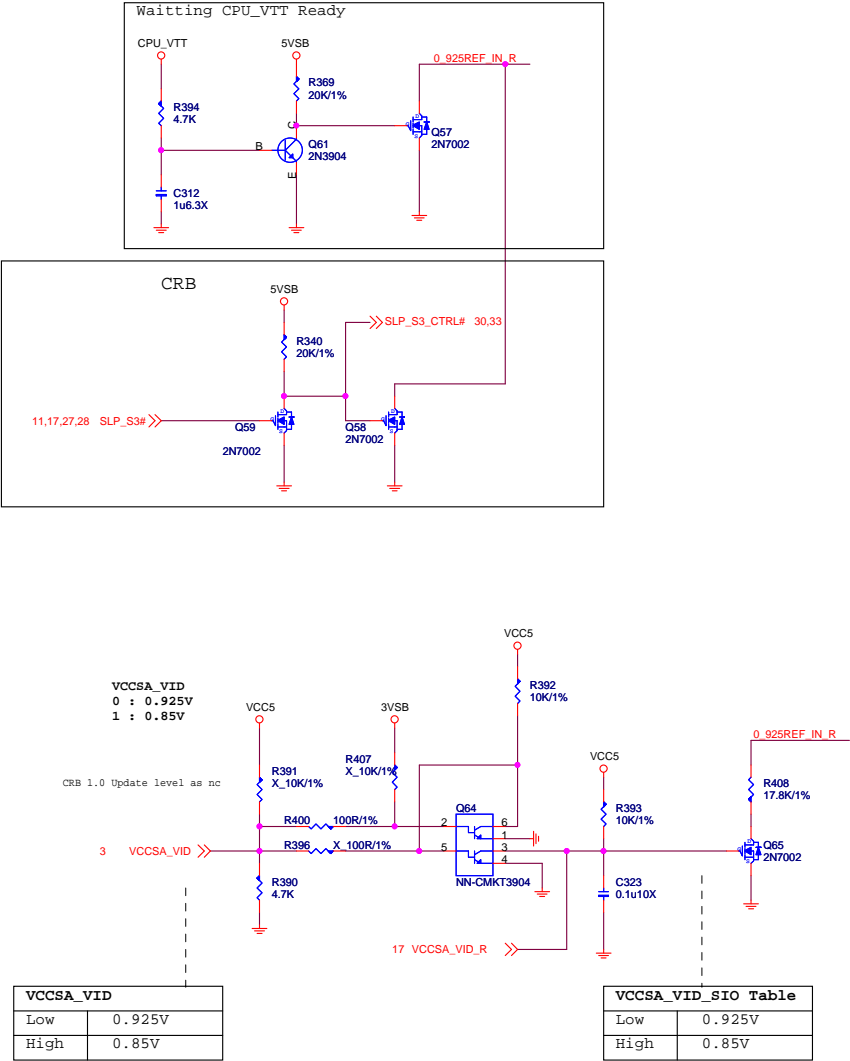
MICRO-STAR INT'L CO.,LTD

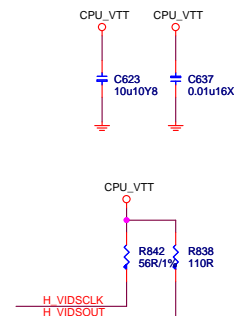
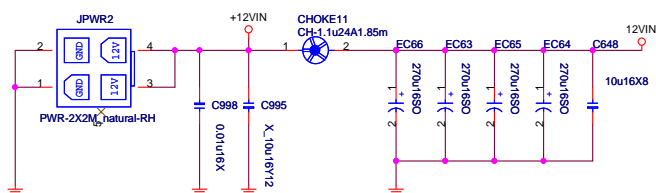
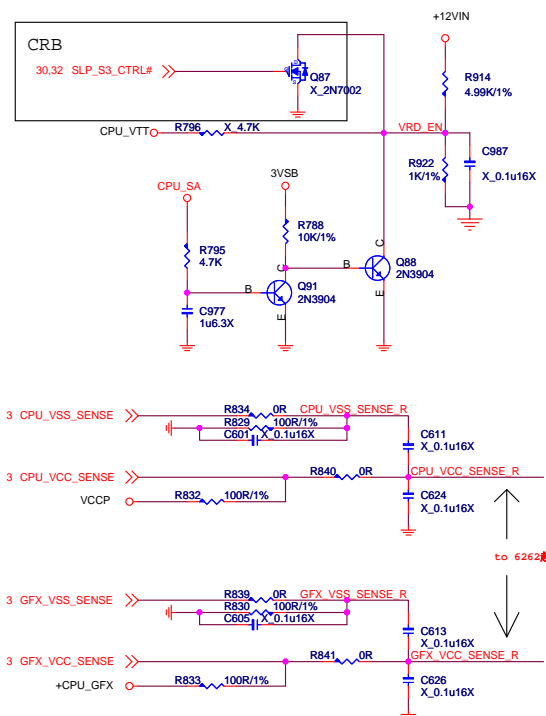
MS-7680

Size Custom	Document Description CPU_VTT - uP6103- 1-Phase	Rev 5.2
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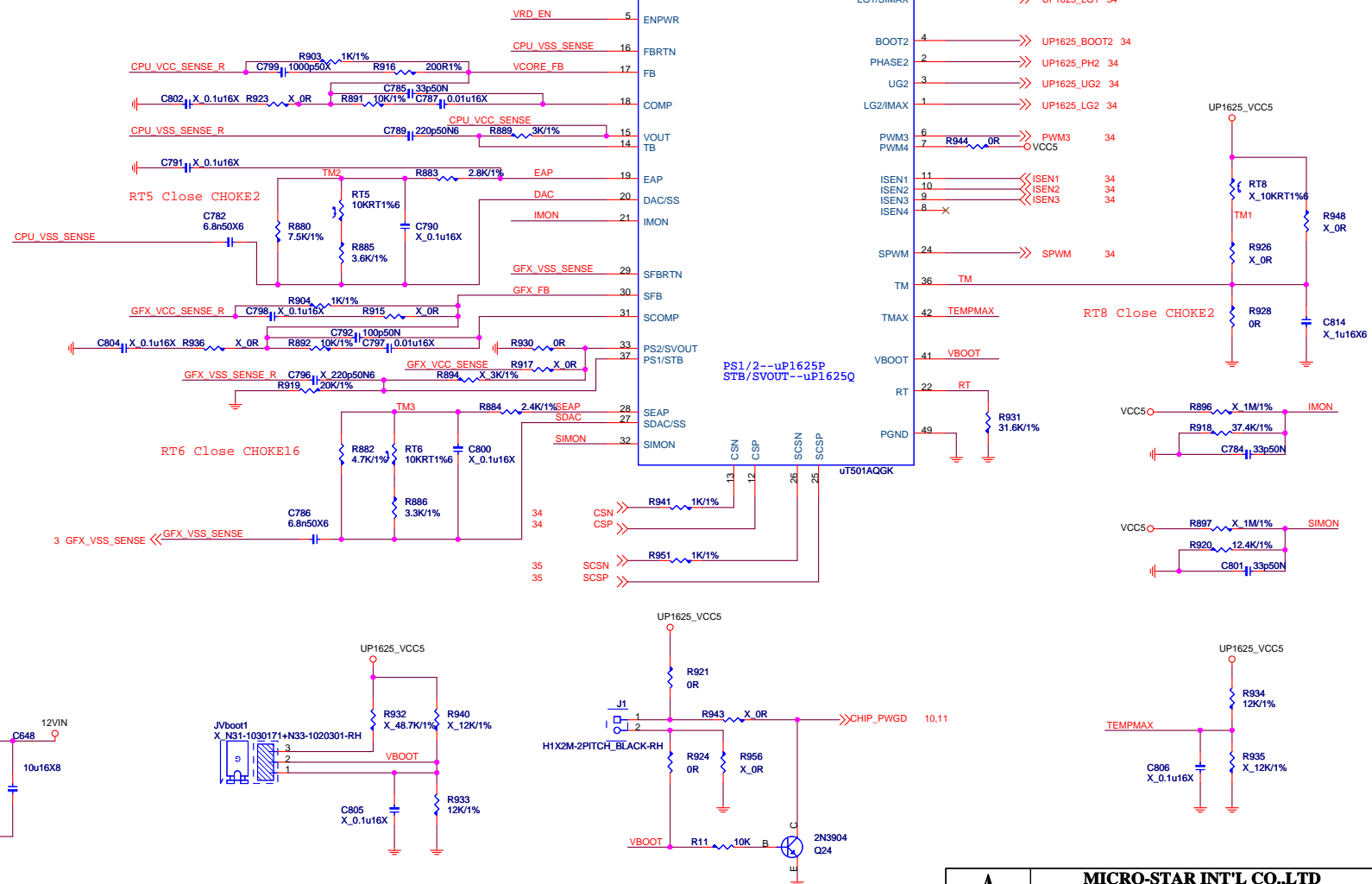
CPU_SA:0.925/0.85

SA Core =8.8A





3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND



```
Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24
```

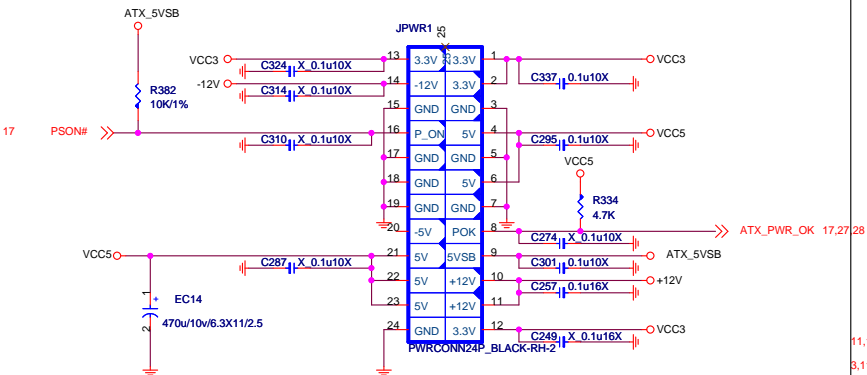


MICRO-STAR INT'L CO.,LTD

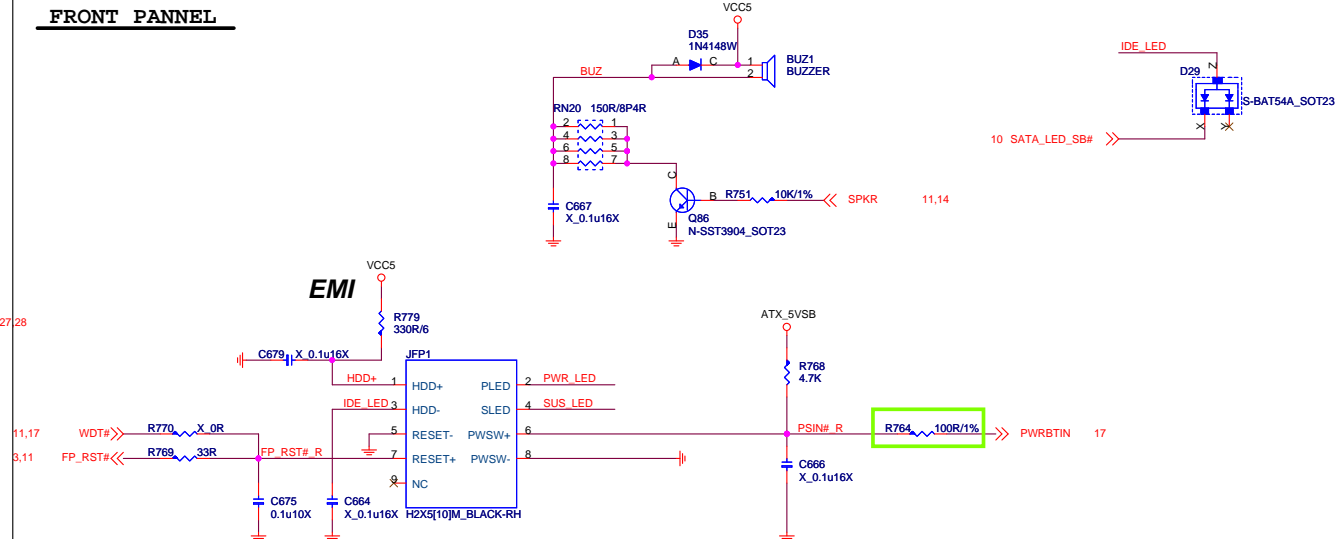
MS-7680

Size Custom	Document Description VRD12 - UPI6234 6+1-Phase	Rev 5.2
Date: Tuesday, September 06, 2011		Sheet 33 of 39

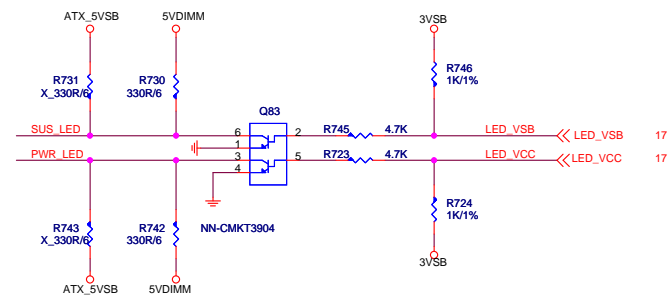
ATX POWER CONNECTOR



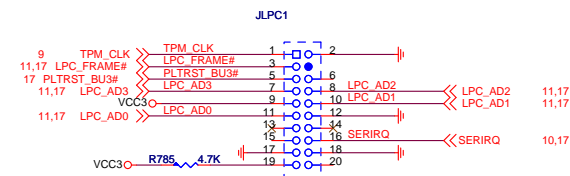
FRONT PANNEL



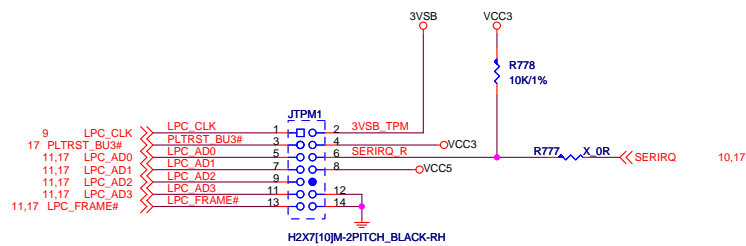
LED (for Fintek 71869)



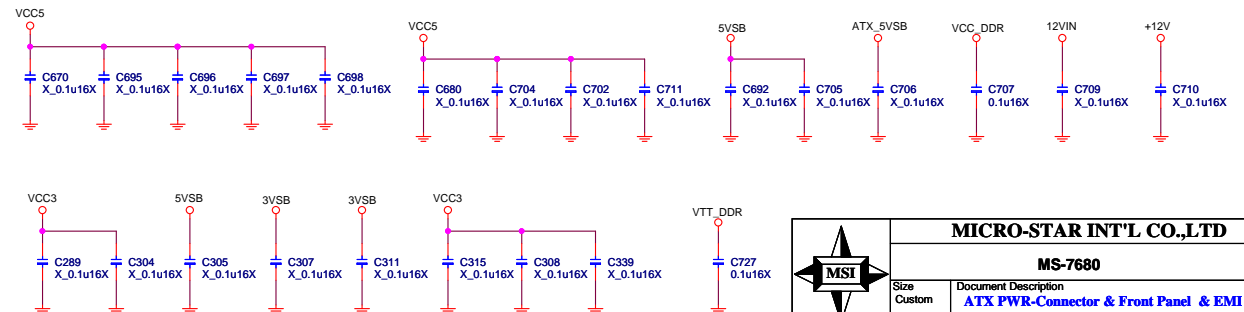
JLPC



TPM/JLPC



EMI



MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description
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Custom	ATX PWR-Connector & Front Panel & EMI	5.2
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OPT	Configure	BOM	Function
A	H61M-P30 (B3)	601-7680-300	H61M-P30 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,Gb Lan, 4*SATAII,10*USB2.0,HD 8Ch Audio,DVI/D-sub,All Solid Cap,EuP,RoHS
B	H61M-P20 (B3)	601-7680-20S	H61M-P22 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,10/100 Lan, 4*SATAII,10*USB2.0,HD 8Ch Audio(3 hole),DVI/D-sub,Half Solid Cap,EuP,RoHS
C	H61M-P25 (B3)	601-7680-310	H61M-P25 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,Gb Lan, 4*SATAII,10*USB2.0,HD 8Ch Audio(3 hole),DVI/D-sub,Half Solid Cap,EuP,RoHS
D	H61M-P22 (B3)	601-7680-320	H61M-P22 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,10/100 Lan, 4*SATAII,10*USB2.0,HD 8Ch Audio(3 hole),DVI/D-sub,Half Solid Cap,EuP,RoHS

Diagram illustrating three network interface cards (NICs) connected to a switch:

- U101:** LAN (RTL8105E-VL-CG)
- R10000:** LAN (510R)
- LAN USB100:** LAN (10/100+USB Con.)

SATA10_11

SATA CON.

SATA14PM_BEIGE-ST-RH

AUDIO10

AUDIO

PK/GR/BU/GY/OR/BL

R20000

AUDIO

75R

EC200
270uF160S

EC201
100u16SO

EC202
470u6.3SO

EC203
100u25EL

Figure 1-1 illustrates the structure of a BIOS label. It shows four examples of labels (LA1, LA2, LA4, LA3) and their corresponding addresses and labels. The labels are represented by colored boxes (blue for LA1, LA2, LA4 and red for LA3) containing the address and label text. The labels are: LA1: 801-7680-19S, LABEL; LA2: 801-7680, LABEL; LA4: 801-7680, LABEL; LA3: AMI_BIOS, LABEL, BIOS_LABEL.



BAT1_X1
+
BAT-BCR

RUB-
USBRUB2
USB

CPU_H1
CPU
鐵座

E21-7557050-L06

HS-PCH1

MEC1 X MEC1

MFC2 X MEC2

HS-0405590-R1



Size Custom	Document Description XDP / Manual Parts	Rev 5.2
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